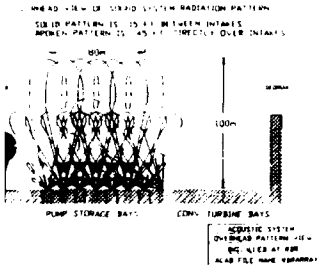
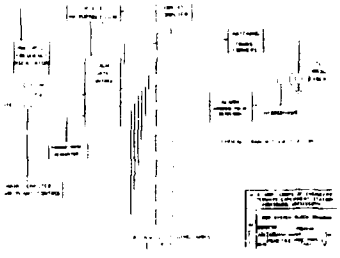
INSTRUCTION REPORT O-91-1

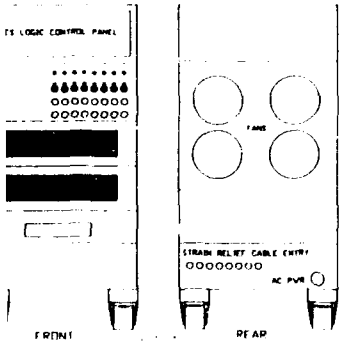
US Army Corps of Engineers

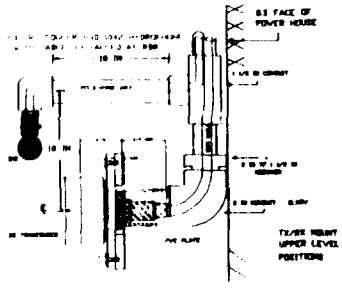
OPERATION AND MAINTENANCE MANUAL, ULTRASONIC FISH DETERRENT SYSTEM





S-16 POWER AMPLIFIER





by

James L. Pickens

Instrumentation Services Division

DEPARTMENT OF THE ARMY
Waterways Experiment Station, Corps of Engineers
3909 Halls Ferry Road, Vicksburg, Mississippi 39180-6199

July 1991
Final Report

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	July 1991	Final report

4. TITLE AND SUBTITLE

Operation and Maintenance Manual, Ultrasonic Fish Deterrent System

5. FUNDING NUMBERS

6. AUTHOR(S)

James L. Pickens

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

USAE Waterways Experiment Station, Instrumentation Services Division, 3909 Halls Ferry Road, Vicksburg, MS 39180-6199

8. PERFORMING ORGANIZATION REPORT NUMBER

Instruction Report O-91-1

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

Available from National Technical Information Service, 5285 Port Royal Road, Springfield, VA 22161.

12a. DISTRIBUTION / AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The Ultrasonic Fish Deterrent system, developed at Waterways Experiment Station, Vicksburg, Mississippi, consists of eight underwater transducers powered by eight 2 KVA switching amplifiers. The input signals to these amplifiers are controlled by a microprocessor and signal conditioner, also developed at WES. The timing durations and frequencies are variable, set by an external computer and can be changed to fit the parameters deemed optimum for the conditions found.

This report describes the various circuits, wiring diagrams, and function charts of the control chassis and microprocessor located in the console as well as instructions for changing the parameters with a computer.

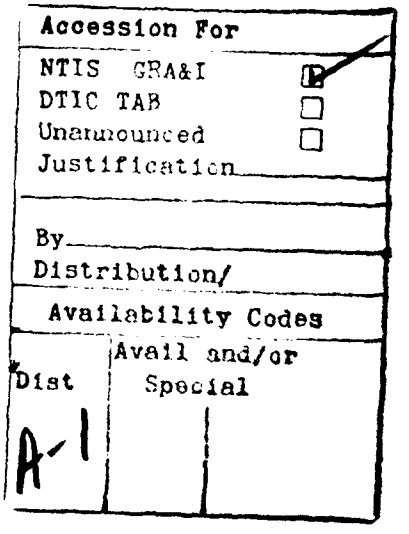
14. SUBJECT TERMS	15. NUMBER OF PAGES
Fishery management--Instruments Ultrasonic transducers	61
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED		

Preface

This report describes a fish deterrent system developed at the US Army Engineer Waterways Experiment Station (WES) by James L. Pickens, Instrumentation Services Division (ISD). Chief of ISD was George P. Bonner.

Commander and Director of WES was COL Larry B. Fulton, EN. Technical Director was Dr. Robert W. Whalin.



Contents

OPERATION AND MAINTENANCE MANUAL, ULTRASONIC FISH DETERRENT SYSTEM

Introduction

The Ultrasonic Fish Deterrent (UFD) system, developed at Waterways Experiment Station, Vicksburg, Mississippi, consists of eight underwater transducers powered by eight 2 KVA switching amplifiers. The input signals to these amplifiers are controlled by a microprocessor and signal conditioner, also developed at WES. The timing durations and frequencies are variable, set by an external computer and can be changed to fit the parameters deemed optimum for the conditions found.

Since simultaneous transmissions result in field cancellation within the transmitted array, the transducers are sequentially triggered, producing a traveling acoustic field (Figure 1). Each transducer has its own impedance matching circuit, so that equal peak pulses will produce equal power out (Figure 2). It has been found during experimentation that frequent pulse signals are as effective as continuous sine waves. Therefore, the main power signals consist of bursts of high frequency energy lasting from 1-5 msec (0.001 sec to 0.005 sec) occurring at up to 20 pulses per second (Figure 3).

The system is designed so that operation can be totally automatic (with preselected pulse rates, frequencies, time intervals) or manually controlled with a computer at the location of the console (Figure 4). The UFD will ultimately be turned on and off by the main computer in the power plant control room, in the automatic mode.

The underwater transmitters are quartz crystal transducers, made by International Transducer Corp. of Santa Barbara, CA (Figure 5). The model No. ITC3003G is cut to resonate at between 112 KHz and 116KHz, although it will respond somewhat past these frequencies. It is driven by 1 KVA pulses from a 2 KVA power amplifier built by Instruments, Inc., of San Diego, CA. Eight of these amplifiers are sequentially enabled to drive eight separate transducers (Figure 6). These signals consist of approximately 118 KHz, 125 KHz, 132 KHz. The time each amplifier is on, and the frequency transmitted during this interval, are adjustable and are

controlled by a preset condition from the microprocessor. An external computer is used to change any of the preset conditions of operation.

A hydrophone (receiver transducer) is placed in the immediate vicinity of the underwater transmitter to monitor its signals (Figure 7) If a malfunction should occur, an alarm is activated at the console, and the red light corresponding to that channel is turned on, advising the operator as to which one is not functioning properly.

The following is a description of the various circuits, wiring diagrams, and function charts of the control chassis and microprocessor located in the console as well as instructions for changing the parameters with a computer.

Transmitter Section

The transmitter section of the system consists of the International Transducer Corporation (ITC) Model 3003G underwater transducer, driven by an Instruments, Inc., amplifier, Model S11-16A, controlled by the WES logic control system.

The following is an explanation of the control system, including the main oscillator, sequence controller, gate control, and incremental gain control.

Oscillator Board 1 (Figure 8)

The main oscillator, Board 1 (Figure 8), consists of three separate oscillators adjustable for three separate frequencies (F1, F2, F3). These frequencies are selected by commands from the micro, energizing one of three relays on the oscillator card. F1 will be adjusted to some frequency around 118 KHz, F2 to about 124 KHz, and F3 to about 132 KHz. These frequencies can be monitored at test points on the front panel and on the printed circuit card.

Since the only way to change the amplitude of the power output signal is by changing the phase angle between the positive and negative inputs at the power amplifier, some modification of the oscillator signal is necessary. The method used to do this is readily seen in the RBRBLK2.DWG (Figure 9). By using three pairs of complimentary one-shot multivibrators on the RBRPHASE board (Figure 10) the separate oscillator signals are changed to narrow pulses, so the gain can be changed by varying the pulse width, while maintaining the frequency. The pulse width will be 1 usec, 2 usec, 3 usec for 15 sec each, respectively, for Gain 1, Gain 2, Gain 3. This will allow a "slow start" each time the system is activated, so no damage to the nearby fish will be done due to instantly being subjected to full power. The slow start will ensure the system operates at 10%, 25%, 66% of full power for 15 seconds each before full power is applied. The gain select commands originate in the microprocessor. The full power output level of the transmitter must be set at the power amplifier.

Phase Board (Board 2)

The phase board (Figure 10) changes the oscillator signal to narrow pulses for a step-up incremental gain sequence. The control to each pair of one-shots is supplied by a TTL pulse, activated by a gain select signal from the microprocessor. A Gain 1 select signal applies 5v to U2 and U3 (pin 5). The RC networks are set for 1 usec. The positive going edge of the oscillator will trigger U2, resulting in a 1 usec pulse at pin 4. The negative going edge of the oscillator signal will trigger U3, resulting in a 1 usec pulse at pin 2. These pulses are routed to the BNC output connectors, ultimately to the + and - inputs at the power amplifier. Each pair of one-shots are selected by Gain 1, 2, or 3 and result in 1, 2, or 3 usec pulses, resulting in 10%, 25%, 66% of full power out. Overall wiring diagram is found in Figure 22.

Logic Control Board (Board 3, Board 4, Figure 11)

The RBRLOGIC Board (Board 3, 4) (Figure 11) takes the oscillator signal, properly phased, and allows the signal to be sequentially applied to the power amplifier inputs. When the master timer signal from the microprocessor (T1 or T2) is on, the And gate U7A allows the phased oscillator signal to be applied simultaneously to And gates U3 and U4. The microprocessor supplies sequentially occurring gates to the And circuit so that the amplifiers work sequentially. Board 3 is for the positive amplifier inputs, Board 4 is for the negative amplifier inputs. All power amps are gated on simultaneously by T1 or T2 (see RBRBLK2.DWG) (Figure 9).

Amplifier Gate

The power amplifiers are enabled when a TTL level voltage is applied to the gate connector J-27 with T1 or T2 on.

Amplifier

Although the total amplifier is explained in the Operation and Maintenance manual, the following paragraph gives a simplified overall explanation of the Instruments, Inc. switching amplifier, Model S11-16A.

The amplifier system is actually eight separate amplifiers, each with a common maximum power output, adjusted by R12, the lower trimpot on the power control board (extreme right side of the upper bay). + 250 volts between TP2 on this card and chassis will produce a maximum output of 2.5 KW. This potentiometer should be adjusted to < 220 VDC max. at TP2 to keep from overranging the transducers. Final adjustment should be made to provide 0.5 vrms max at the front panel BNC (2 mv/v). With the proper matching transformer at the transducer, this should produce a power output of 1 KW RMS. Each amplifier channel is separate and can be operated singly by enabling only the one monitored at the front panel. The output adjustment must be made with the enable switch on and the load connected. The amplifier will not work unless the gate input to the amplifier is high (+5v TTL level).

Do not operate the amp very long with the air filters removed. This will result in overheating.

Matching Network

Each transducer cable is connected to a step-up transformer and choke coils. This will allow the amplifier to match the 50 ohm cable (RG-8 coax) with a lower voltage on the long cable. Since each channel has a high capacitive reactance due to the long cable (33 pf/ft) and a quartz transducer (4500 pf nom.), a 50 ohm transformer will allow matching, regardless of the cable length. Another transformer with a 50 ohm primary and 1:7.2 step-up ratio is placed in a box above the transducer (Figure 12). This allows full power to be restored at the top of each transducer with little loss due to cable capacitance. Together with choke coils equal to approximately 240 uH and parallel capacitors, the reactance of the transducer is virtually cancelled (Figure 13).

Each channel is individually tuned with the matching inductor and capitors in parallel with the transducers. The best compromise frequency, resulting in minimum reflected power, is 122 KHz. This setting allows the system to be operated at 119 KHz - 126 KHz with less than 10% power loss. With output transformers having selectable turns ratios, the individual channels could be tuned to reduce or eliminate refelcted power altogether.

Transducer

The system uses the ITC 3003G underwater transducer, a quartz crystal, resonant at 112 KHz. These transducers are located 4 ft above each draft tube and 15 ft deep halfway between each tube (Figure 14). A total of eight transducers are installed to produce an acoustic field in front of the pump-back tubes. The lower transducers (Figure 15) are mounted at a +11 degrees angle to beam up along a 1:5 slope on the bottom of the tailrace (Figure 16). The complete description and specs are contained in the additional manufacturers manual.

Receiver

A hydrophone, ITC Model 1127, is mounted in the vicinity of each transmitter, picking up a portion of the transmitted signal (Figure 7). This signal is routed through the RBRAMP card (Figure 17) to the missing pulse detector (MPD) board. Each MPD has 4 channels and monitors the presence of a signal during the time T1 or T2 is active (Figure 18). Proper operation is indicated by a green light on the front panel. If a malfunction occurs, that particular green light will go off and its associated red light will come on. Each channel has its own MPD circuit and lights. The red light will remain on as long as that channel is not receiving a signal from that hydrophone during T1 or T2 time (Figure 19).

Microprocessor

The microprocessor requires + 12 volts for operation and contains a converter for +/-12v, +5v operating voltage at approximately 150 ma. It provides internally pre-programmed, specifically timed signals for the various functions required. The schematic and timing chart (Figures 20 and 21) show how this is accomplished and the following is an explanation of its operation. A second micro is supplied as a spare.

Purpose

The purpose of this device is to provide TTL pulses to the UFD. The Rapid Fire Pulse Generator (RFPG) provides this function with 33 outputs and 2 inputs. The outputs consist of two timing signals T1 and T2, 8 signal enables, 8 amplifier enables, 3 oscillator select lines, 3 gain level lines, and 8 missing pulse detector lines. The two inputs consist of an automatic/ manual select line and a computer start pulse line.

Setup

To configure the RFPG in the automatic mode or to operate it in the manual mode a terminal of some type is needed. In most cases an IBM compatible computer with a communications software package will be most convenient; however, any terminal will work.

To begin operation, connect the 36-Pin Centronics cable between the RFPG and the UFD. Next connect power via a Bendix connector to the RFPG. Common is on PIN A and +12 Volts in on PIN D. Next connect the communications cable (TC-4) between the RFPG and the terminal. An ONSET TC-4 cable must be used due to level shifting requirements. The modular end plugs into the RFPG and the DB-25 end connects to the terminal. Power up terminal or put computer in terminal mode. The RFPG communicates at 9600 baud, eight data bits, one stop bit, and no parity. Make sure CAPS LOCK is engaged. Place the power switch on the RFPG in the ON position. When the RFPG is powered up it checks to see whether it is in the manual or automatic mode. Therefore, to switch modes first power switch to OFF, change modes, and then power switch to ON.

Manual Mode Operation

In the manual mode, the user has the option to choose two functions. Selecting Function 1 places the RFPG in the T1 mode. First the user selects an oscillator and then starts and stops rapid fire by pressing S and Q respectively. Pressing X will take the user back to the manual mode menu. Selecting function 2 places the RFPG in a mode where all eight channels are continuously enabled. First the user selects an oscillator and then starts and stops continuous enable by pressing S and Q respectively. Pressing X will take the user back to the manual mode menu.

Automatic Mode Operation

In the automatic mode, the user enters predetermined values for:

T1

T2

TIME BETWEEN T1 and T2

TIME BETWEEN T2 AND NEXT T2

TIME ON FOR EACH OSCILLATOR

Oscillators select lines, one through three, will be fired sequentially and will be free running regardless of the state of T1 and T2. Once the values have been entered, the RFPG goes into a holding pattern where it waits for a computer start pulse or an S key from the terminal. Once the computer start pulse line goes high or the S key is pressed the RFPG follows through its timing sequence. The RFPG continues operation until the Q key is pressed or the computer start pulse line goes low depending on how the procedure was started. Upon completion, the RFPG displays the previous inputs and falls back into its holding pattern. To change the predetermined inputs, the user must power switch to OFF and then reapply power.

In the event of a power failure, the +12 volts to the micro is routed through a Time Delay Relay (TDR) to allow the computer time to boot up before power is applied to the microprocessor (approximately 1.5 minutes).

Power

The power required for the system is 240 volt, single phase at 30 A. A 5 KVA isolation 480 volt, transformer is used to step down the 480 volts available to 240 volts with a 110v outlet to supply AC for the electronics. The microprocessor power is supplied by a 12 volt battery, permanently connected to a battery charger through a TDR.

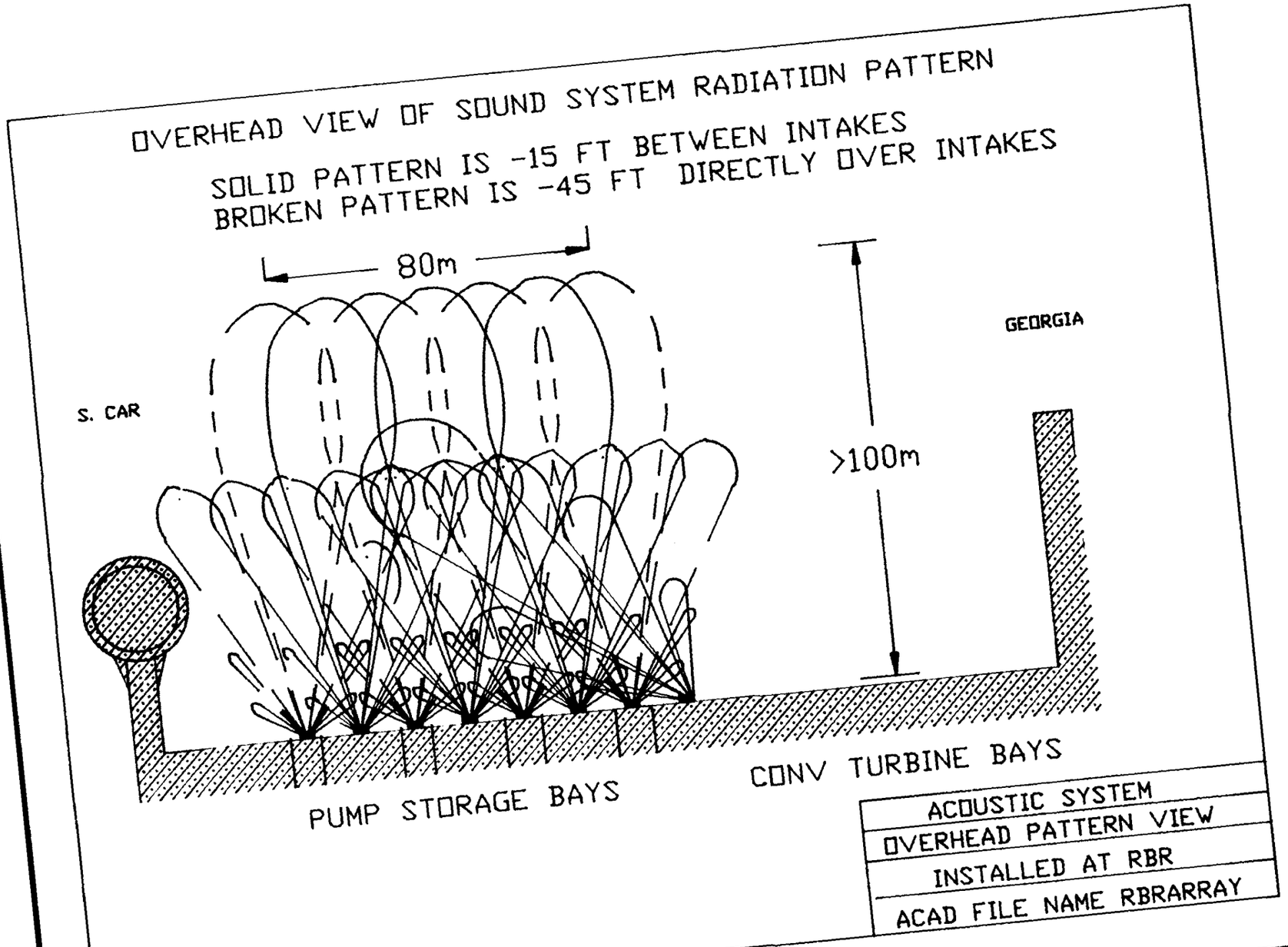

OVERHEAD VIEW OF SOUND SYSTEM RADIATION PATTERN
SOLID PATTERN IS -15 FT BETWEEN INTAKES
BROKEN PATTERN IS -45 FT DIRECTLY OVER INTAKES
80m
>100m
S. CAR
GEORGIA
PUMP STORAGE BAYS
CONV TURBINE BAYS
ACOUSTIC SYSTEM
OVERHEAD PATTERN VIEW
INSTALLED AT RBR
ACAD FILE NAME RBRARRAY

FIG. 1

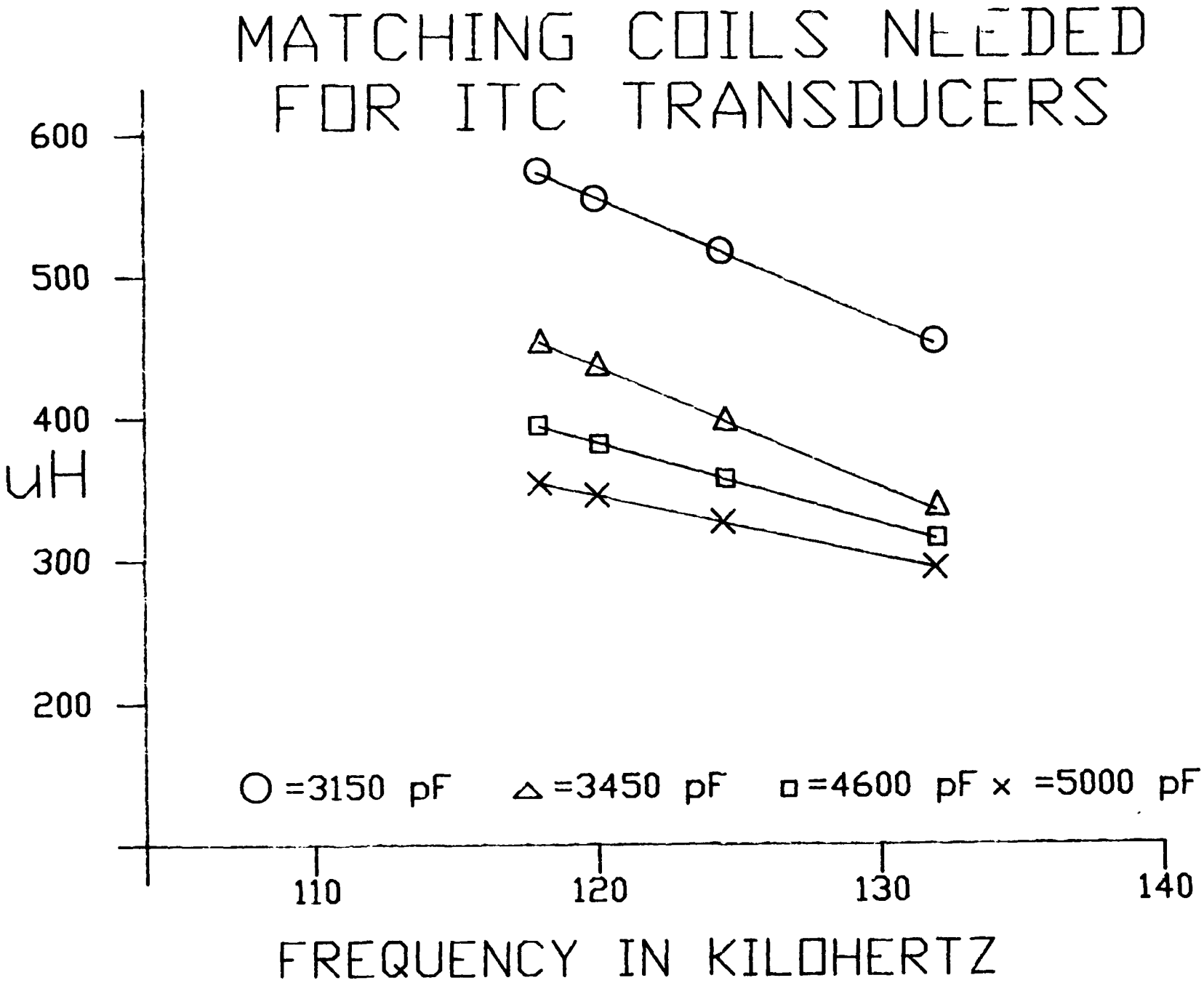
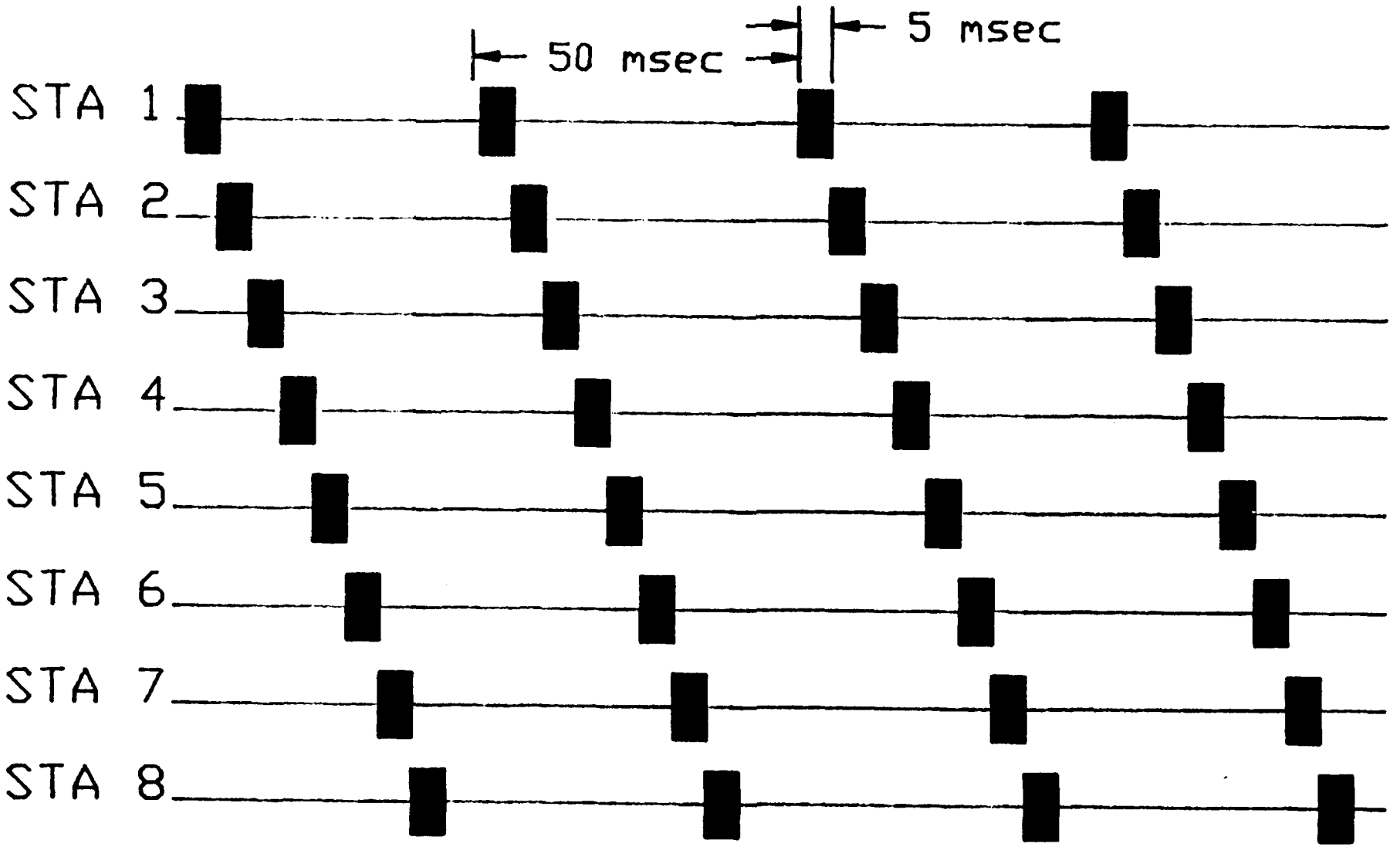

MATCHING COILS NEEDED
FOR ITC TRANSDUCERS
600
500
400
300
200
uH
O =3150 pF
△ =3450 pF
□ =4600 pF
x =5000 pF
110
120
130
140
FREQUENCY IN KILOHERTZ

FIG. 2



SEQUENTIAL FIRING__STATIONS 1-8
HI FREQ BURSTS @ 10% DUTY CYCLE
RICHARD B RUSSELL DAM

FIG. 3

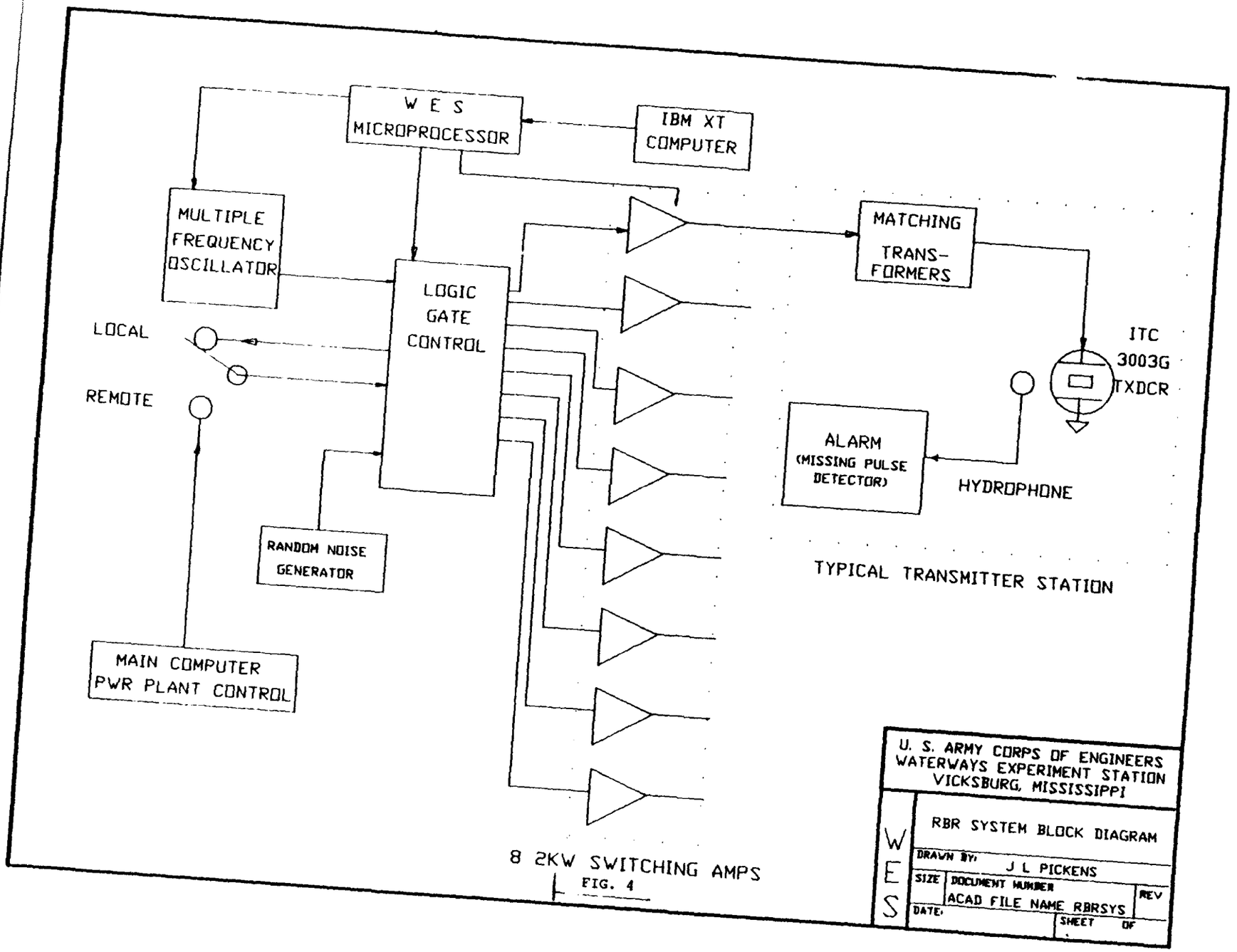

W E S
MICROPROCESSOR
IBM XT
COMPUTER
MULTIPLE
FREQUENCY
OSCILLATOR
LOGIC
GATE
CONTROL
MATCHING
TRANS-
FORMERS
LOCAL
REMOTE
ITC
3003G
TXDCR
ALARM
(MISSING PULSE
DETECTOR)
HYDROPHONE
RANDOM NOISE
GENERATOR
TYPICAL TRANSMITTER STATION
MAIN COMPUTER
PWR PLANT CONTROL
8 2KW SWITCHING AMPS
U. S. ARMY CORPS OF ENGINEERS
WATERWAYS EXPERIMENT STATION
VICKSBURG, MISSISSIPPI
W
E
S
RBR SYSTEM BLOCK DIAGRAM
DRAWN BY: J L PICKENS
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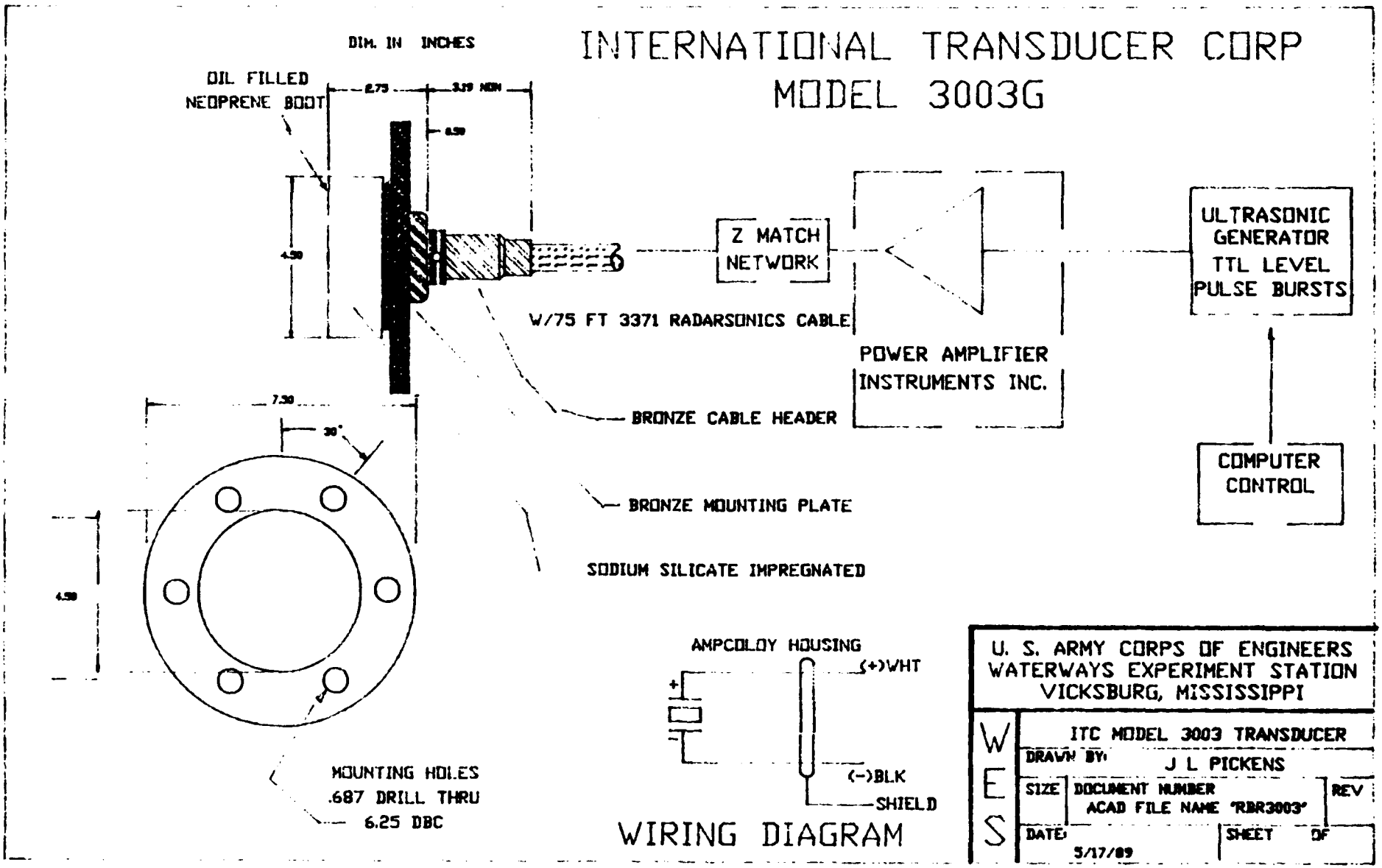
FIG. 4


DIM. IN INCHES
INTERNATIONAL TRANSDUCER CORP
MODEL 3003G
OIL FILLED
NEOPRENE BOOT
6.75
3.19 MIN
6.50
4.50
7.50
30°
4.50
Z MATCH
NETWORK
W/75 FT 3371 RADARSONICS CABLE
POWER AMPLIFIER
INSTRUMENTS INC.
ULTRASONIC
GENERATOR
TTL LEVEL
PULSE BURSTS
COMPUTER
CONTROL
BRONZE CABLE HEADER
BRONZE MOUNTING PLATE
SODIUM SILICATE IMPREGNATED
MOUNTING HOLES
.687 DRILL THRU
6.25 DBC
AMPCOLOY HOUSING
(+)WHT
(-)BLK
SHIELD
WIRING DIAGRAM
U. S. ARMY CORPS OF ENGINEERS
WATERWAYS EXPERIMENT STATION
VICKSBURG, MISSISSIPPI
W
E
S
ITC MODEL 3003 TRANSDUCER
DRAWN BY: J L PICKENS
SIZE
DOCUMENT NUMBER
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DATE: 5/17/89
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FIG. 5

INSTRUMENTS INC.

S-16 POWER AMPLIFIER

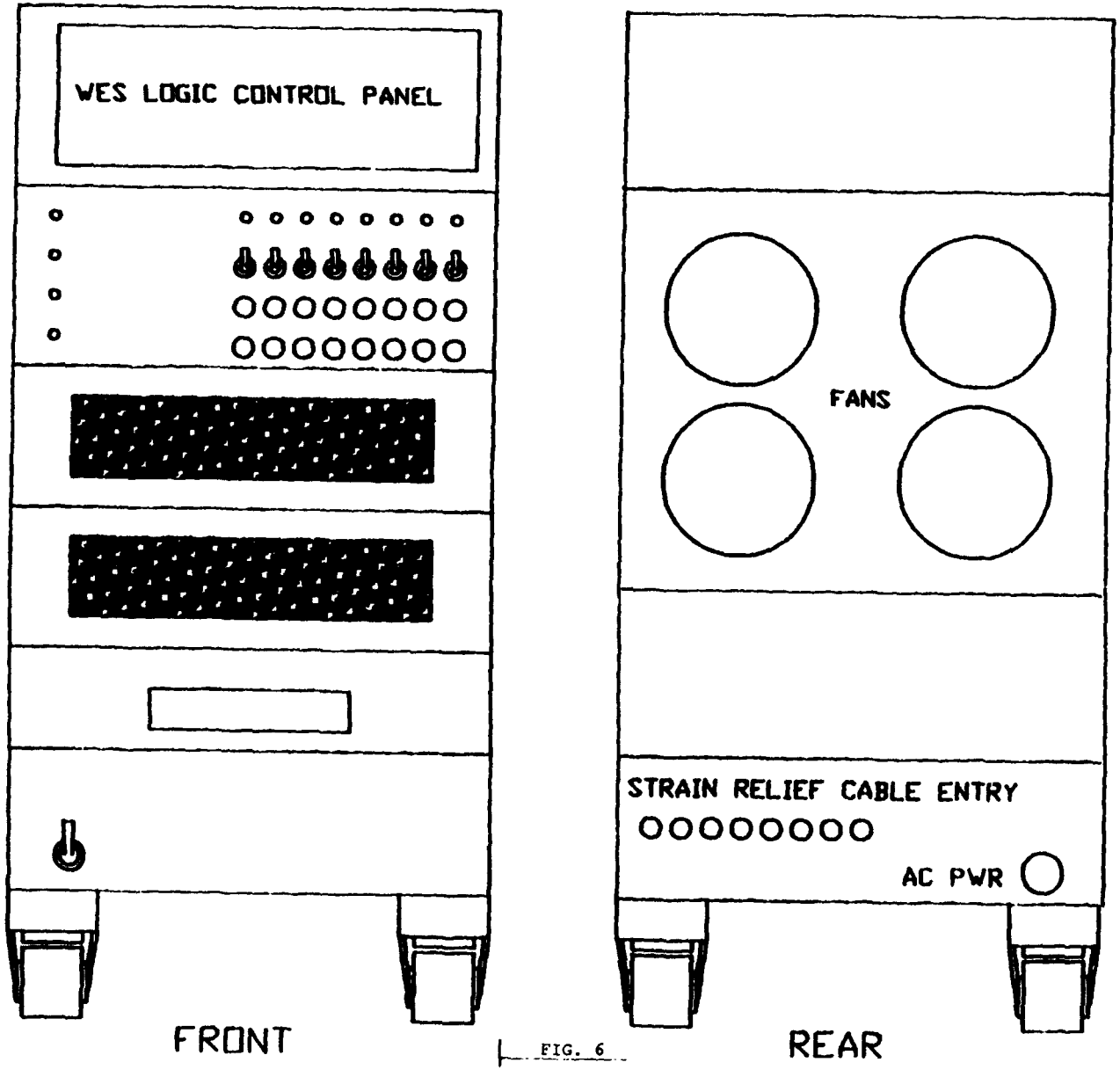

FIG. 6

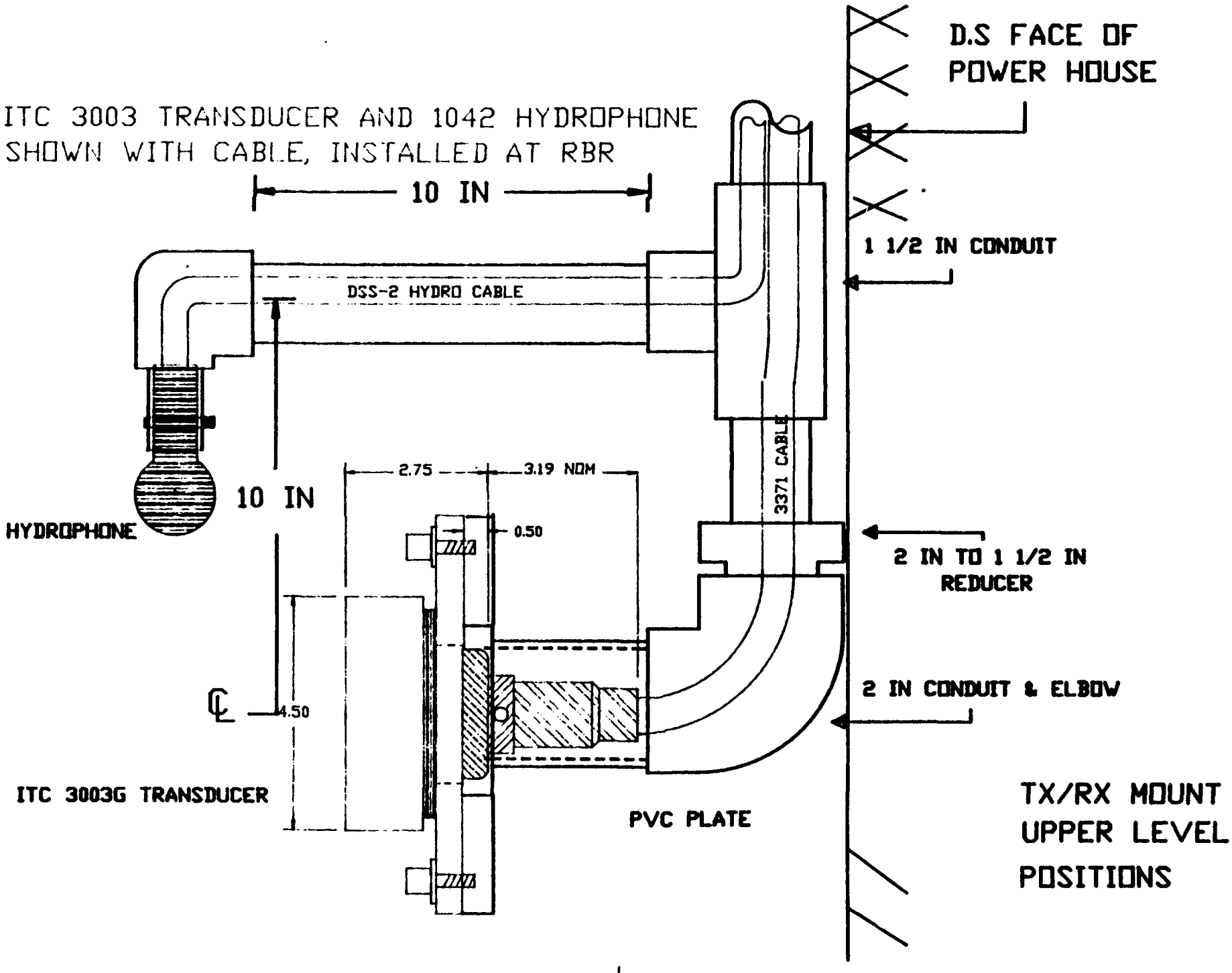
ITC 3003 TRANSDUCER AND 1042 HYDROPHONE
SHOWN WITH CABLE, INSTALLED AT RBR
10 IN
D.S FACE OF
POWER HOUSE
1 1/2 IN CONDUIT
DSS-2 HYDRO CABLE
3371 CABLE
10 IN
HYDROPHONE
2.75
3.19 NOM
0.50
2 IN TO 1 1/2 IN
REDUCER
2 IN CONDUIT & ELBOW
4.50
ITC 3003G TRANSDUCER
PVC PLATE
TX/RX MOUNT
UPPER LEVEL
POSITIONS

FIG. 7

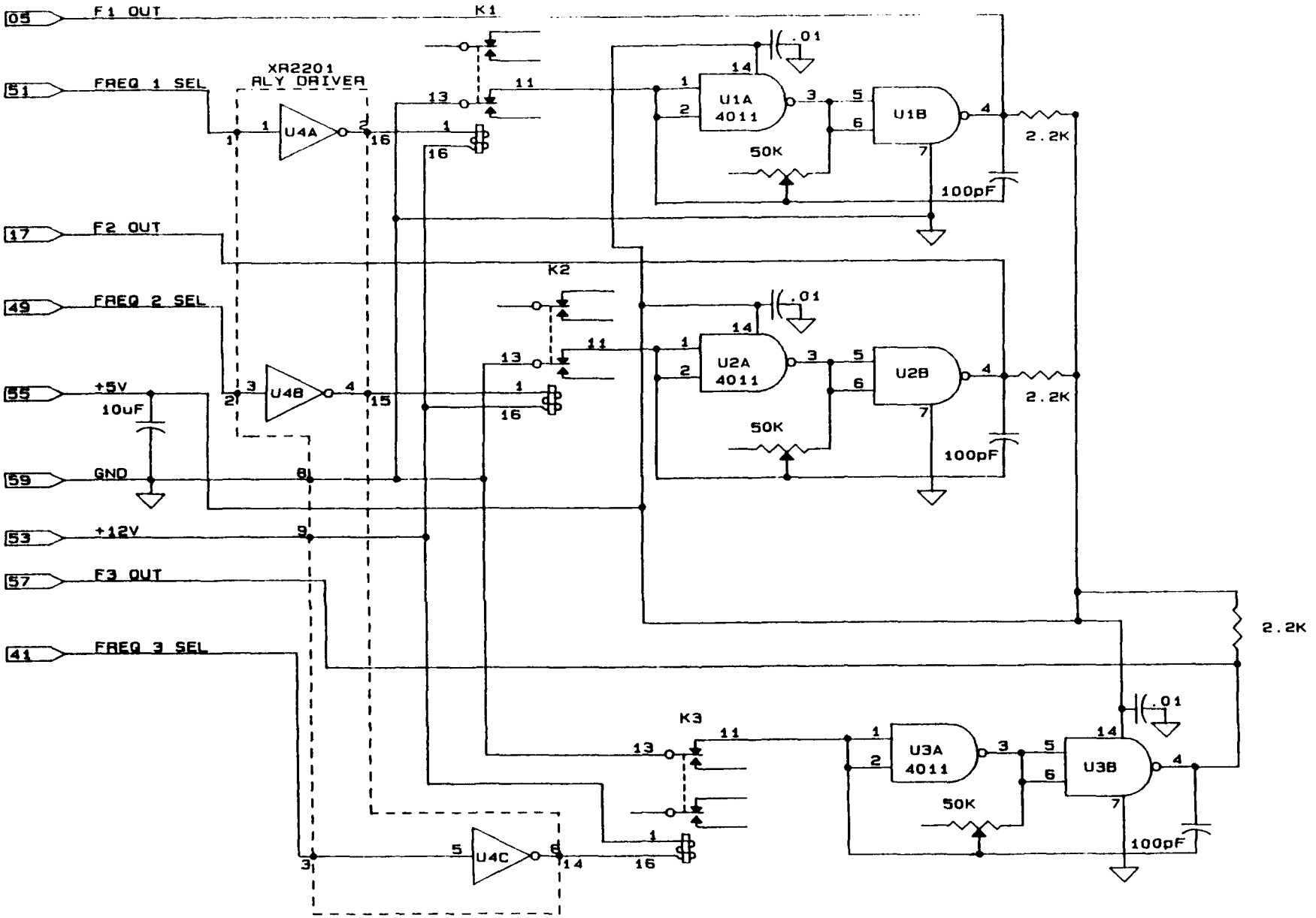

FIG. 8

RBR OSCILLATOR BOARD		
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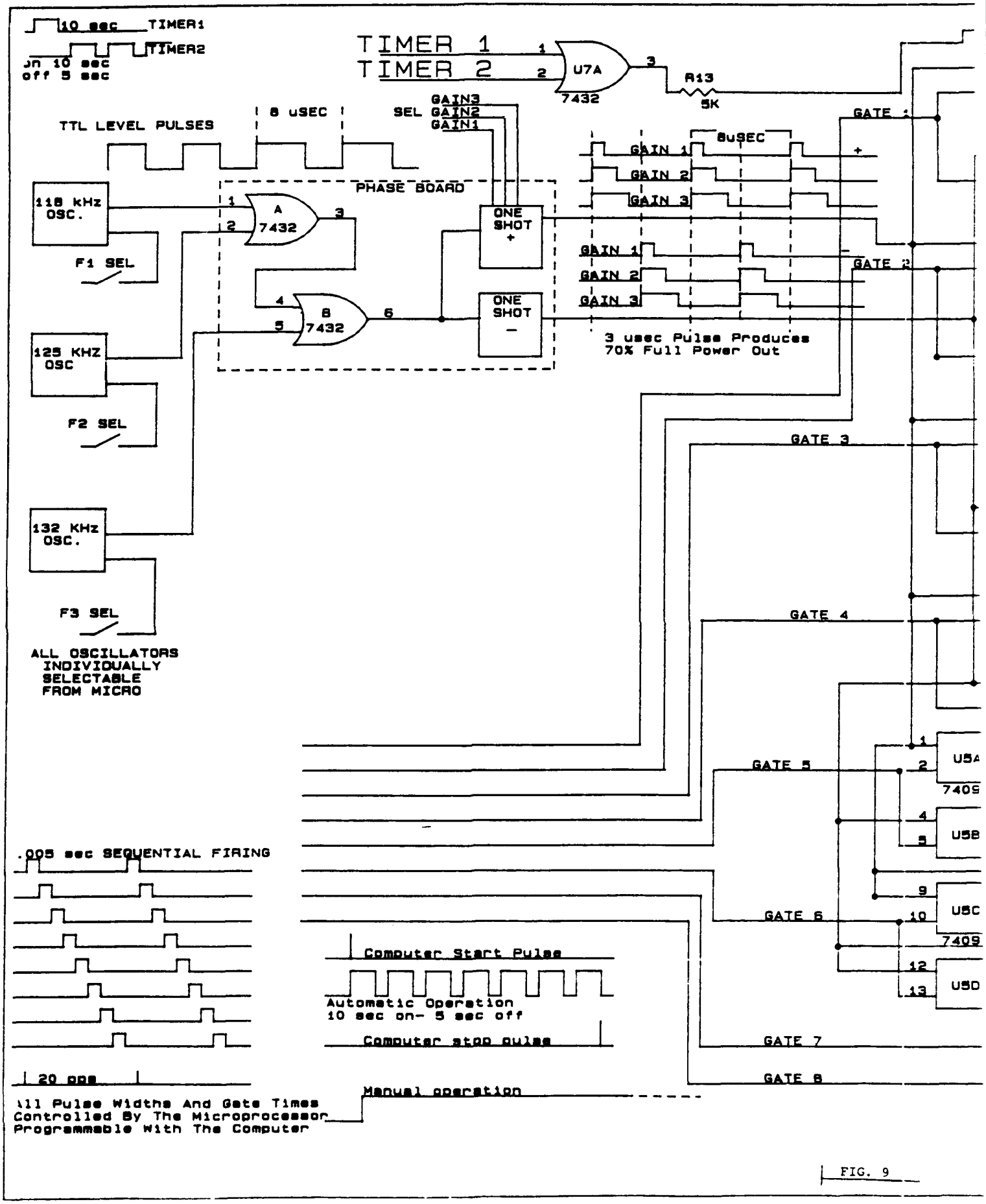
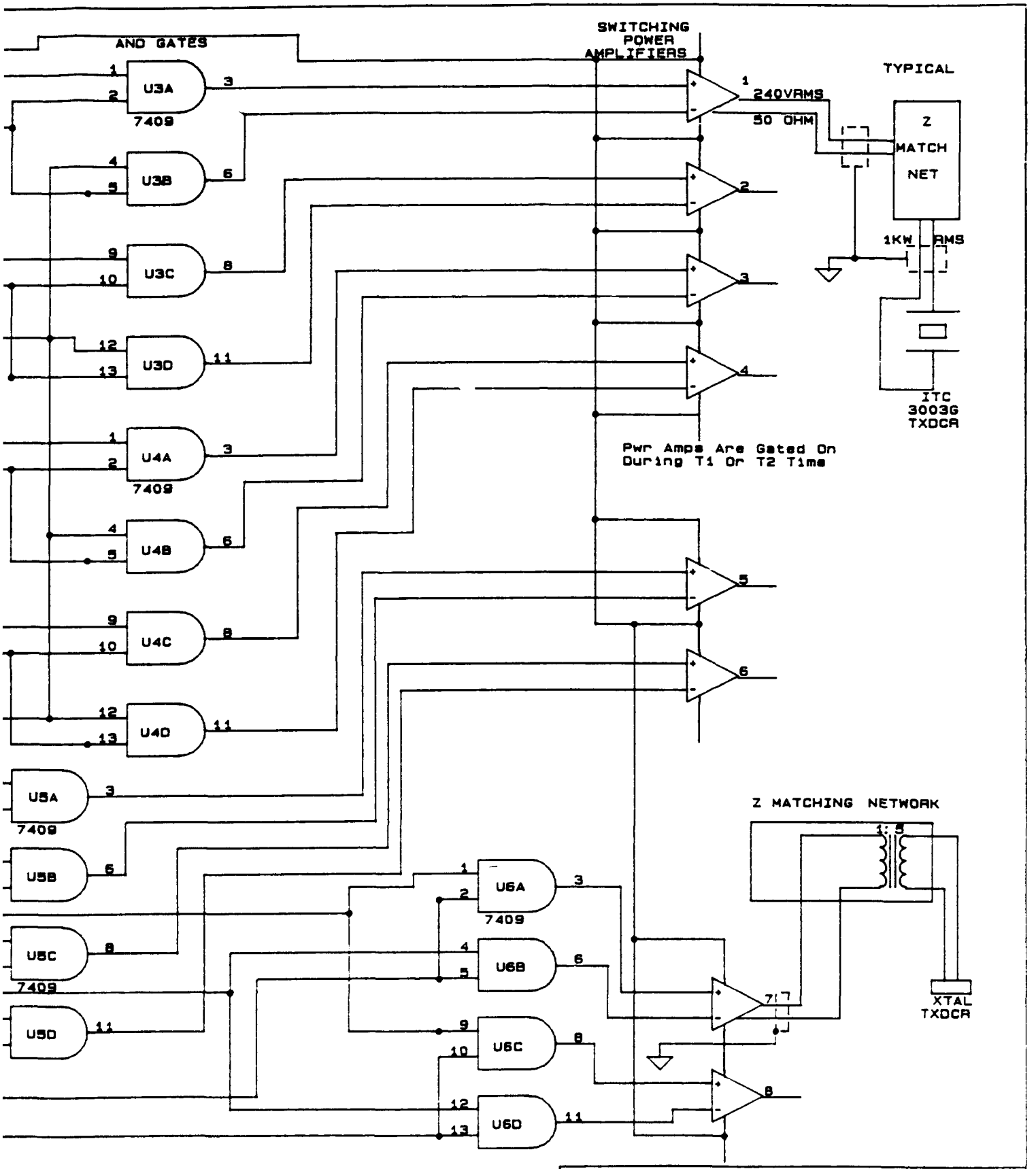

10 sec TIMER1
TIMER2
on 10 sec
off 5 sec
TIMER 1
TIMER 2
U7A
7432
R13
5K
GAIN3
SEL GAIN2
GAIN1
TTL LEVEL PULSES
8 uSEC
PHASE BOARD
118 kHz OSC.
A
7432
F1 SEL
125 KHZ OSC
B
7432
F2 SEL
132 KHz OSC.
F3 SEL
ONE SHOT +
ONE SHOT -
8uSEC
GAIN 1
GAIN 2
GAIN 3
GATE 1
GATE 2
3 usec Pulse Produces
70% Full Power Out
GATE 3
GATE 4
GATE 5
GATE 6
GATE 7
GATE 8
ALL OSCILLATORS
INDIVIDUALLY
SELECTABLE
FROM MICRO
U5A
7409
U5B
U5C
U5D
.005 sec SEQUENTIAL FIRING
Computer Start Pulse
Automatic Operation
10 sec on- 5 sec off
Computer stop pulse
20 pps
Manual operation
All Pulse Widths And Gate Times
Controlled By The Microprocessor
Programmable With The Computer

FIG. 9



RBR BLOCK DIAGRAM/SEQUENTIAL FIRING SCHEME

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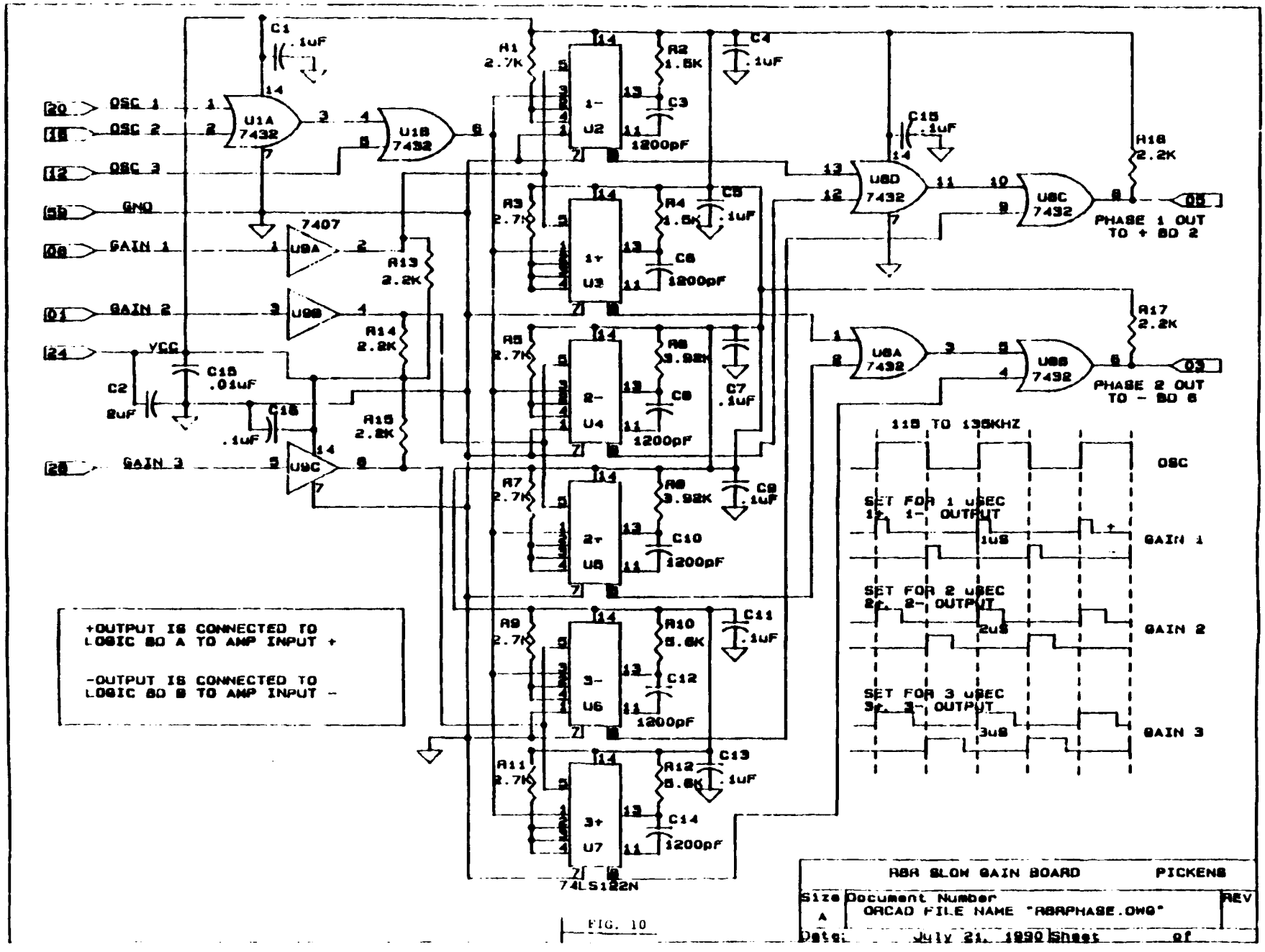

OSC 1
OSC 2
OSC 3
GND
GAIN 1
GAIN 2
GAIN 3
VCC
U1A 7432
U1B 7432
7407
U8A
U8B
U8C
C1 .1uF
C2 2uF
C15 .01uF
C16 .1uF
R13 2.2K
R14 2.2K
R15 2.2K
R1 2.7K
R2 1.5K
C4 .1uF
C3 1200pF
1- U2
R3 2.7K
R4 1.5K
C5 .1uF
C6 1200pF
1+ U3
R5 2.7K
R6 3.92K
C7 .1uF
C8 1200pF
2- U4
R7 2.7K
R8 3.92K
C9 .1uF
C10 1200pF
2+ U5
R9 2.7K
R10 5.6K
C11 .1uF
C12 1200pF
3- U6
R11 2.7K
R12 5.6K
C13 .1uF
C14 1200pF
3+ U7
74LS122N
C15 .1uF
U8D 7432
U8C 7432
R16 2.2K
PHASE 1 OUT TO + SD 2
U8A 7432
U8B 7432
R17 2.2K
PHASE 2 OUT TO - SD 6
115 TO 135KHZ
OSC
SET FOR 1 uSEC 1+, 1- OUTPUT
1uS
GAIN 1
SET FOR 2 uSEC 2+, 2- OUTPUT
2uS
GAIN 2
SET FOR 3 uSEC 3+, 3- OUTPUT
3uS
GAIN 3
+OUTPUT IS CONNECTED TO LOGIC SD A TO AMP INPUT +
-OUTPUT IS CONNECTED TO LOGIC SD B TO AMP INPUT -
RBR SLOW GAIN BOARD
PICKENS
Size A
Document Number
ORCAD FILE NAME "RBRPHASE.DWG"
REV
Date: July 21, 1990 Sheet of

FIG. 10

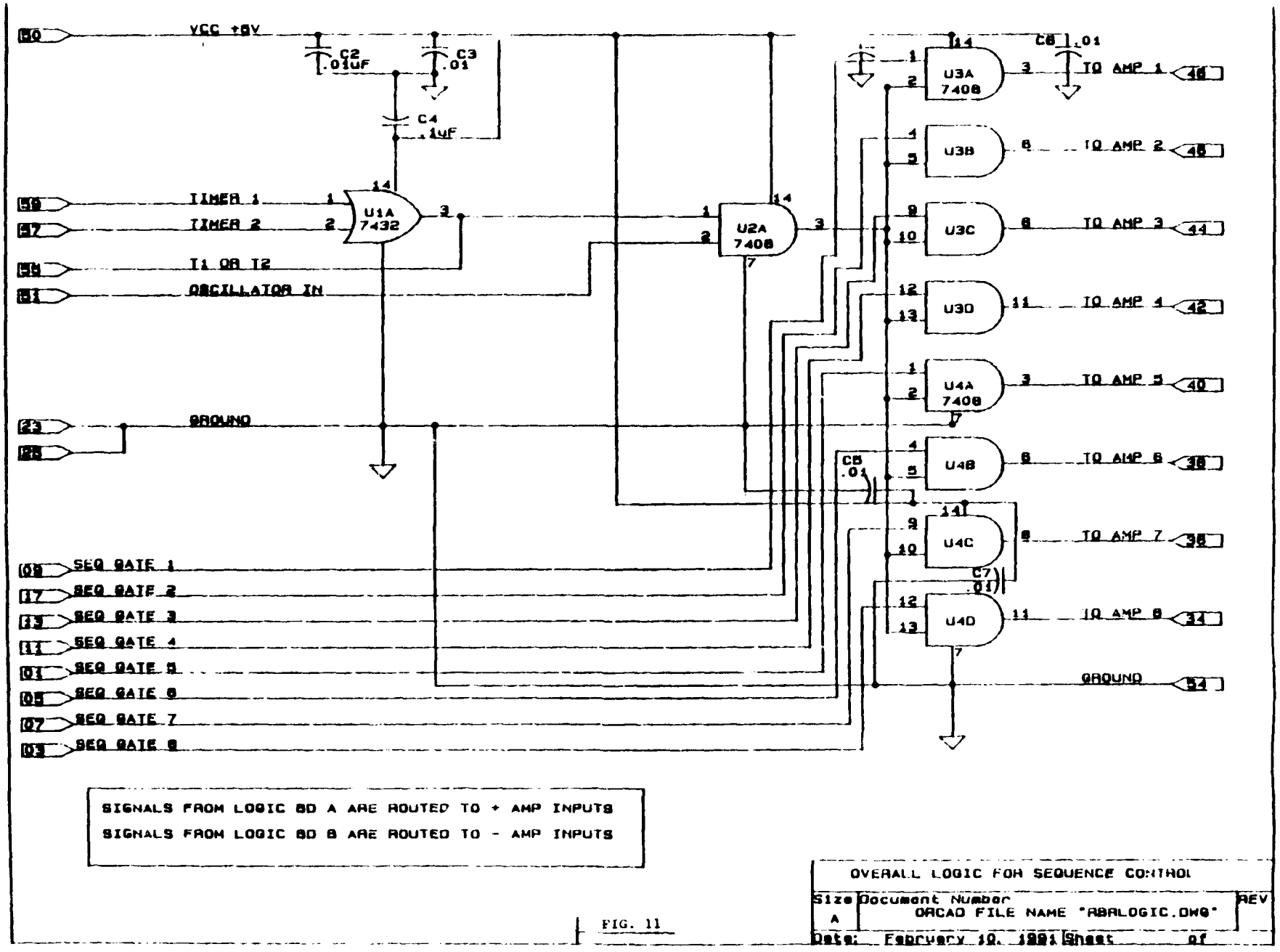

VCC +5V
C2 .01uF
C3 .01
C4 .1uF
TIMER 1
TIMER 2
I1 OR I2
OSCILLATOR IN
GROUND
U1A 7432
U2A 7408
U3A 7408
U3B
U3C
U3D
U4A 7408
U4B
U4C
U4D
C6 .01
C7 .01
C8 .01
C5 .01
IQ AMP 1
IQ AMP 2
IQ AMP 3
IQ AMP 4
IQ AMP 5
IQ AMP 6
IQ AMP 7
IQ AMP 8
SEQ GATE 1
SEQ GATE 2
SEQ GATE 3
SEQ GATE 4
SEQ GATE 5
SEQ GATE 6
SEQ GATE 7
SEQ GATE 8
SIGNALS FROM LOGIC BD A ARE ROUTED TO + AMP INPUTS
SIGNALS FROM LOGIC BD B ARE ROUTED TO - AMP INPUTS
OVERALL LOGIC FOR SEQUENCE CONTROL
Size A
Document Number
ORCAD FILE NAME "RBRLOGIC.DWG"
REV
Date: February 10, 1991 Sheet of

FIG. 11

10 BY 10
BREAKOUT
BOX LOCATED
ON PARAPET
WALL ABOVE
EACH BAY

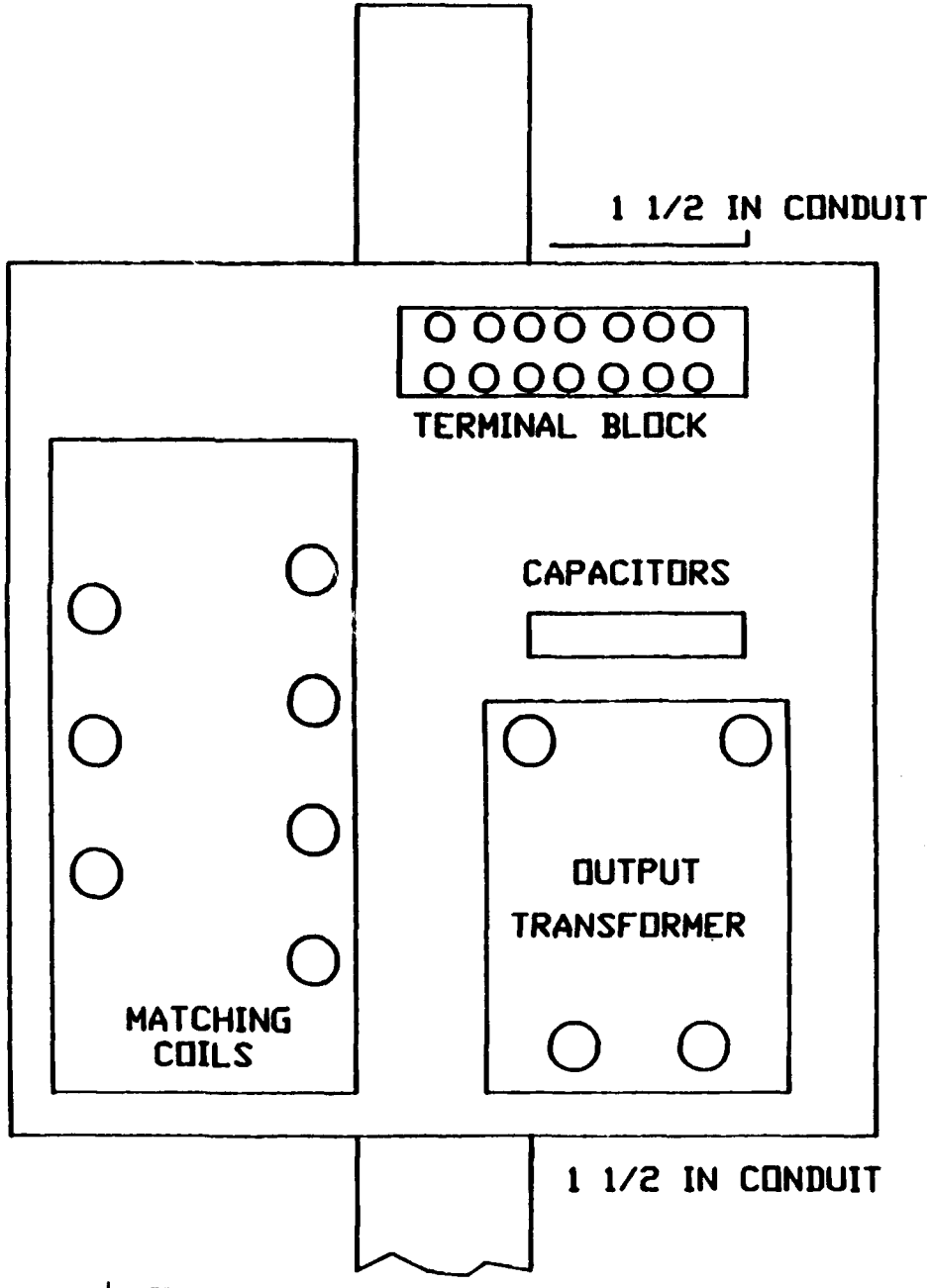


FIG. 12

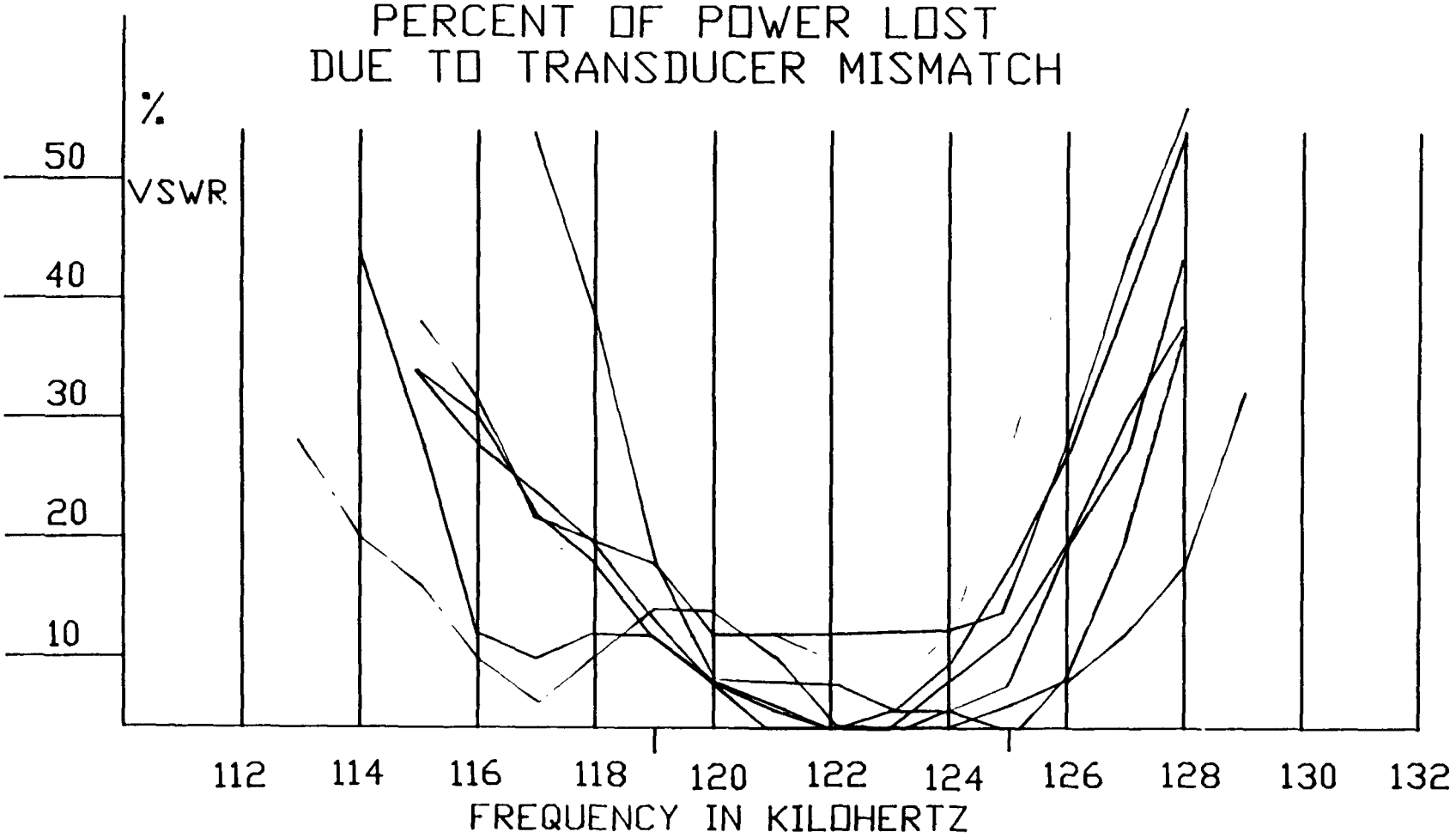

PERCENT OF POWER LOST
DUE TO TRANSDUCER MISMATCH
%
VSWR
50
40
30
20
10
112
114
116
118
120
122
124
126
128
130
132
FREQUENCY IN KILOHERTZ

FIG. 13

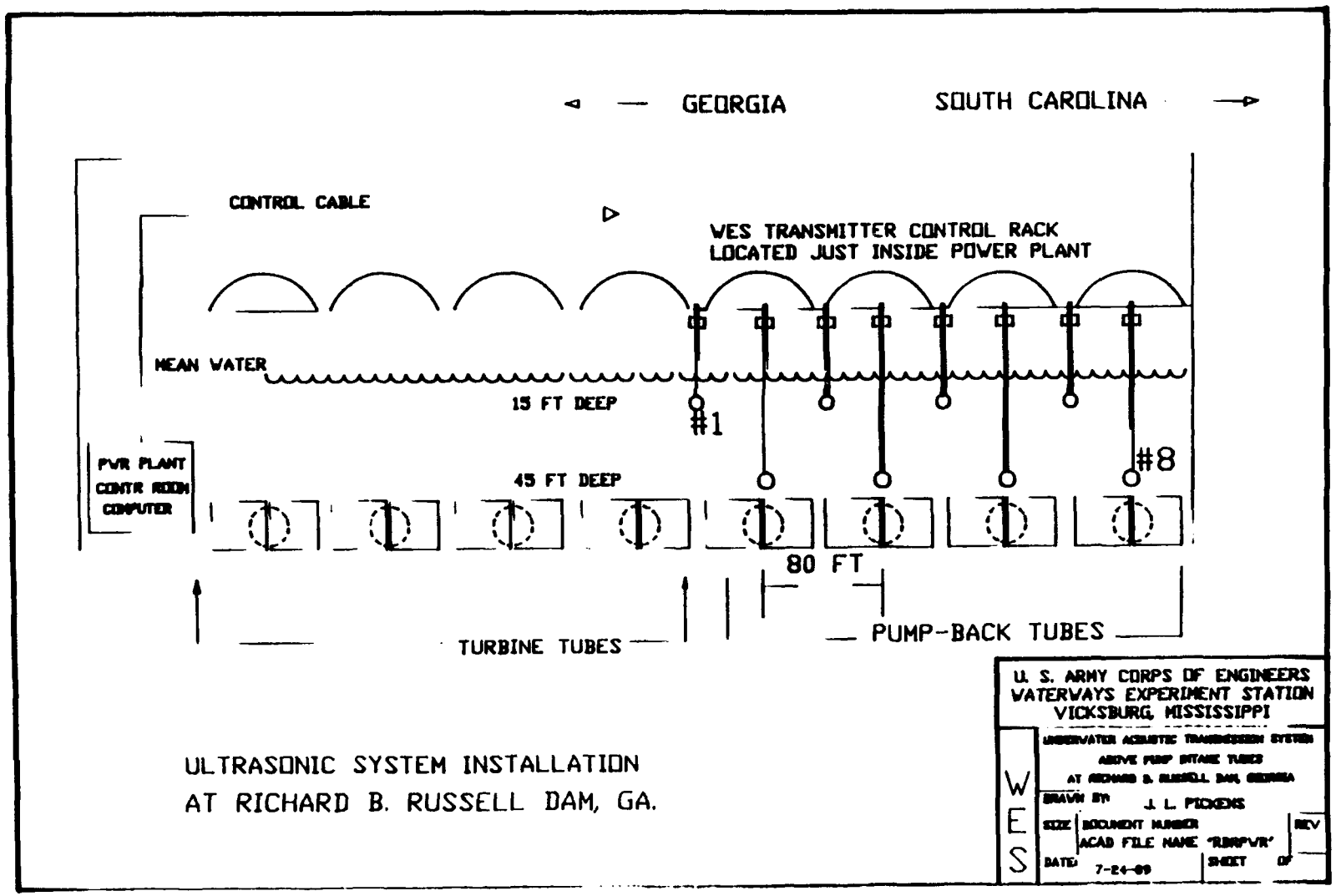

GEORGIA
SOUTH CAROLINA
CONTROL CABLE
WES TRANSMITTER CONTROL RACK
LOCATED JUST INSIDE POWER PLANT
MEAN WATER
15 FT DEEP
#1
#8
PWR PLANT
CONTR ROOM
COMPUTER
45 FT DEEP
80 FT
TURBINE TUBES
PUMP-BACK TUBES
U. S. ARMY CORPS OF ENGINEERS
WATERWAYS EXPERIMENT STATION
VICKSBURG, MISSISSIPPI
W
E
S
DRAWN BY J. L. PICKENS
ACAD FILE NAME "RBRPVR"
DATE 7-24-89
ULTRASONIC SYSTEM INSTALLATION
AT RICHARD B. RUSSELL DAM, GA.

FIG. 14

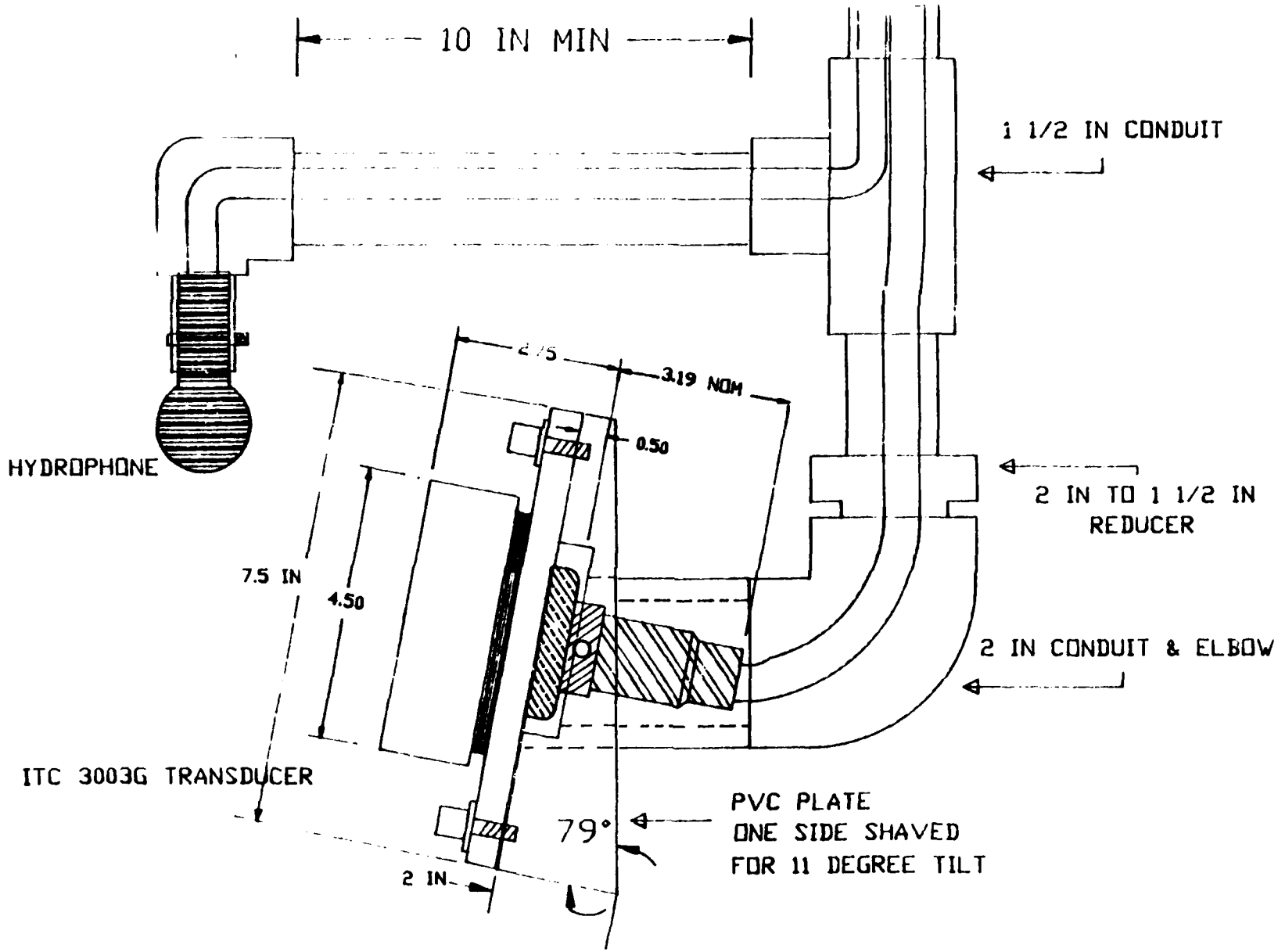
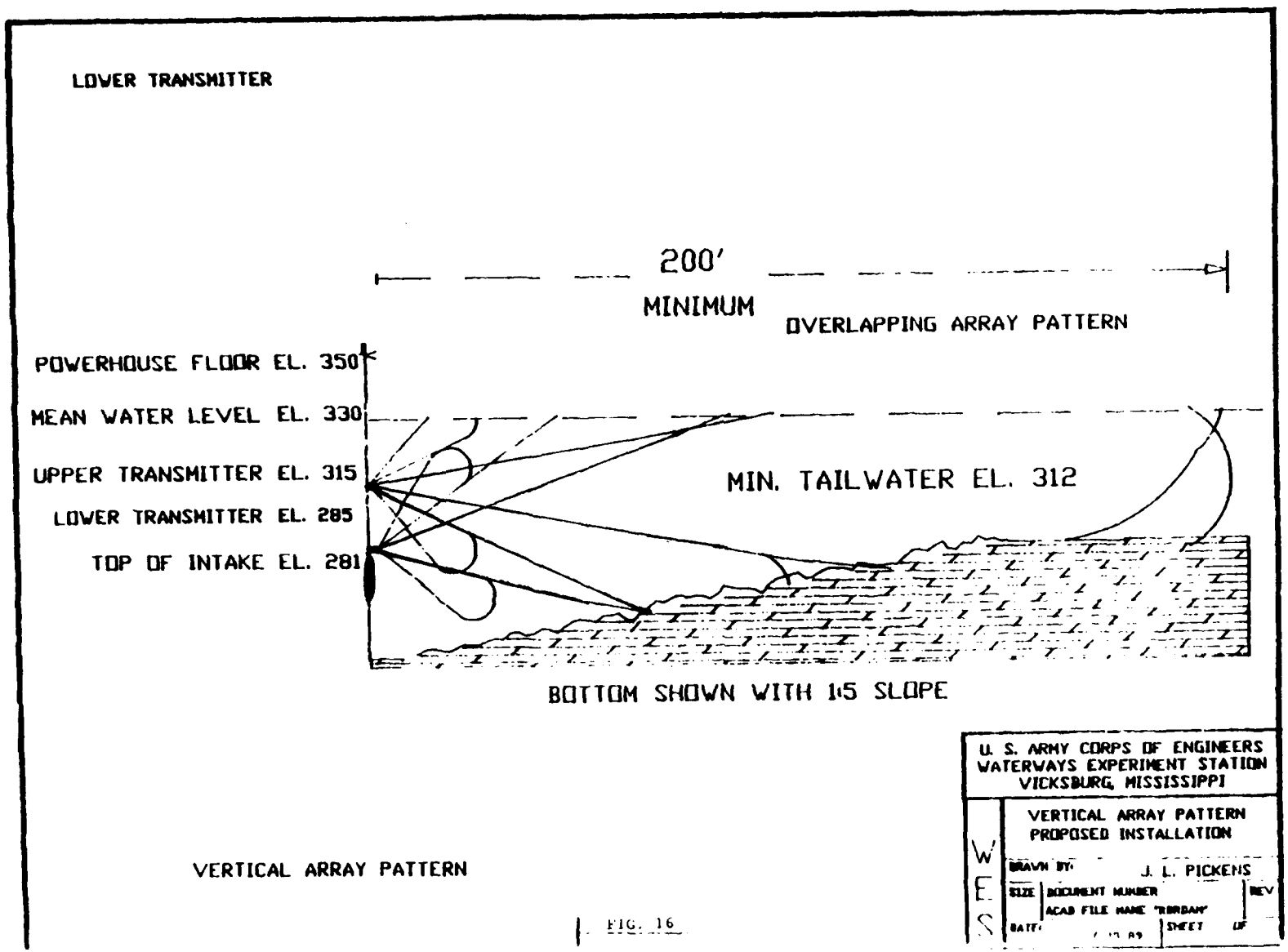

10 IN MIN
1 1/2 IN CONDUIT
HYDROPHONE
2.75
3.19 NOM
0.50
2 IN TO 1 1/2 IN
REDUCER
7.5 IN
4.50
2 IN CONDUIT & ELBOW
ITC 3003G TRANSDUCER
79°
PVC PLATE
ONE SIDE SHAVED
FOR 11 DEGREE TILT
2 IN

FIG. 15



VERTICAL ARRAY PATTERN

FIG. 16

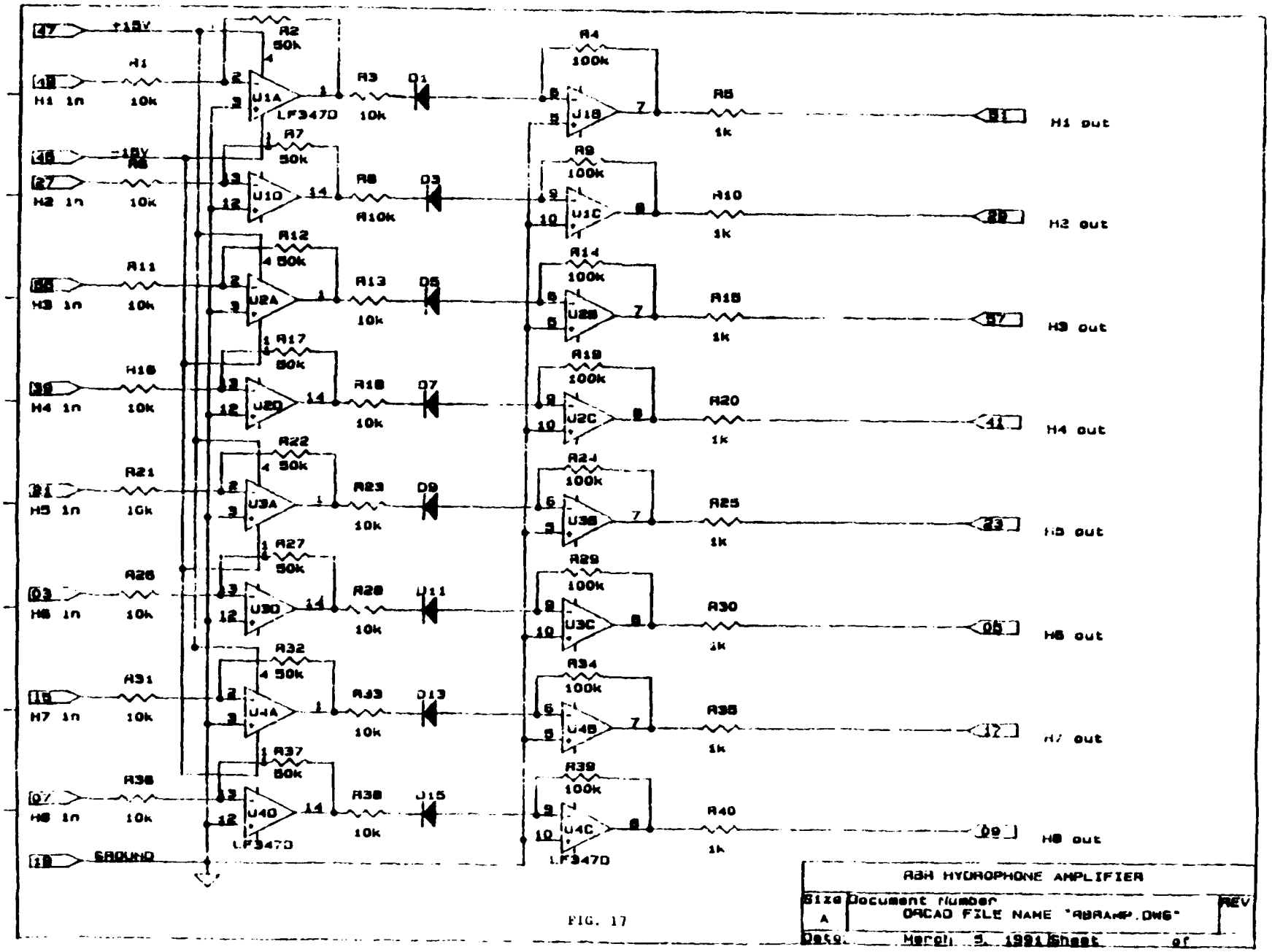

+15V
-15V
GROUND
H1 in
H2 in
H3 in
H4 in
H5 in
H6 in
H7 in
H8 in
H1 out
H2 out
H3 out
H4 out
H5 out
H6 out
H7 out
H8 out
LF347D
R2
R3
R4
R5
R7
R8
R9
R10
R12
R13
R14
R15
R17
R18
R19
R20
R22
R23
R24
R25
R27
R28
R29
R30
R32
R33
R34
R35
R37
R38
R39
R40
D1
D3
D5
D7
D9
D11
D13
D15
U1A
U1B
U1C
U2A
U2B
U2C
U3A
U3B
U3C
U4A
U4B
U4C
A3H HYDROPHONE AMPLIFIER
Size
A
Document Number
ORCAD FILE NAME "A3HAMP.DWG"
REV
Date: March 5, 1991 Sheet of

FIG. 17

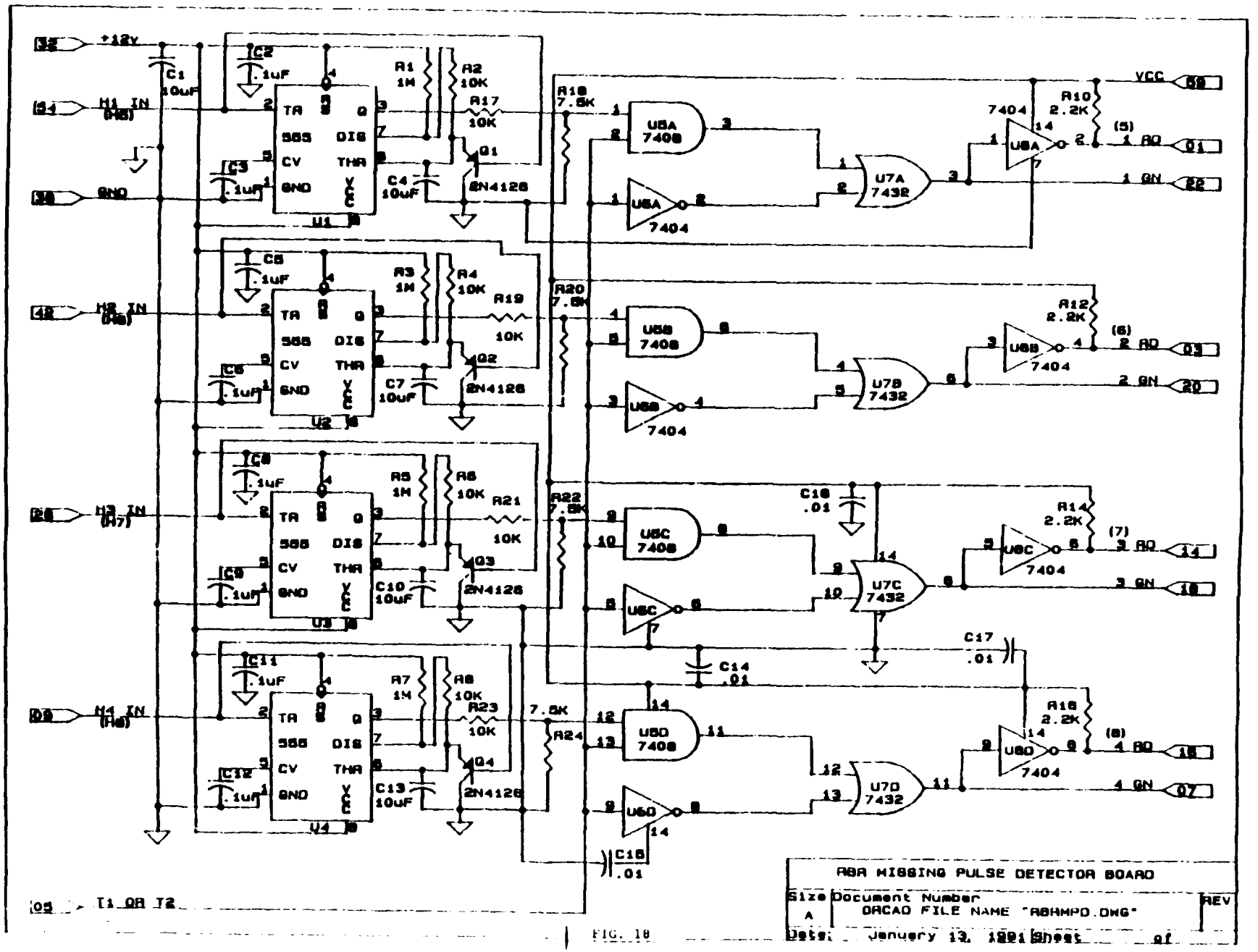

+12v
H1 IN
GND
H2 IN
H3 IN
H4 IN
I1 OR I2
TR
OUT
SSS
DIS
CV
THR
GND
VCC
U1
U2
U3
U4
2N4126
7.5K
7404
7432
VCC
(5) 1 RD
1 GN
(6) 2 RD
2 GN
(7) 3 RD
3 GN
(8) 4 RD
4 GN
RBR MISSING PULSE DETECTOR BOARD
Size A
Document Number
ORCAD FILE NAME "RBRMPD.DWG"
REV
Date: January 13, 1991
Sheet of

FIG. 10

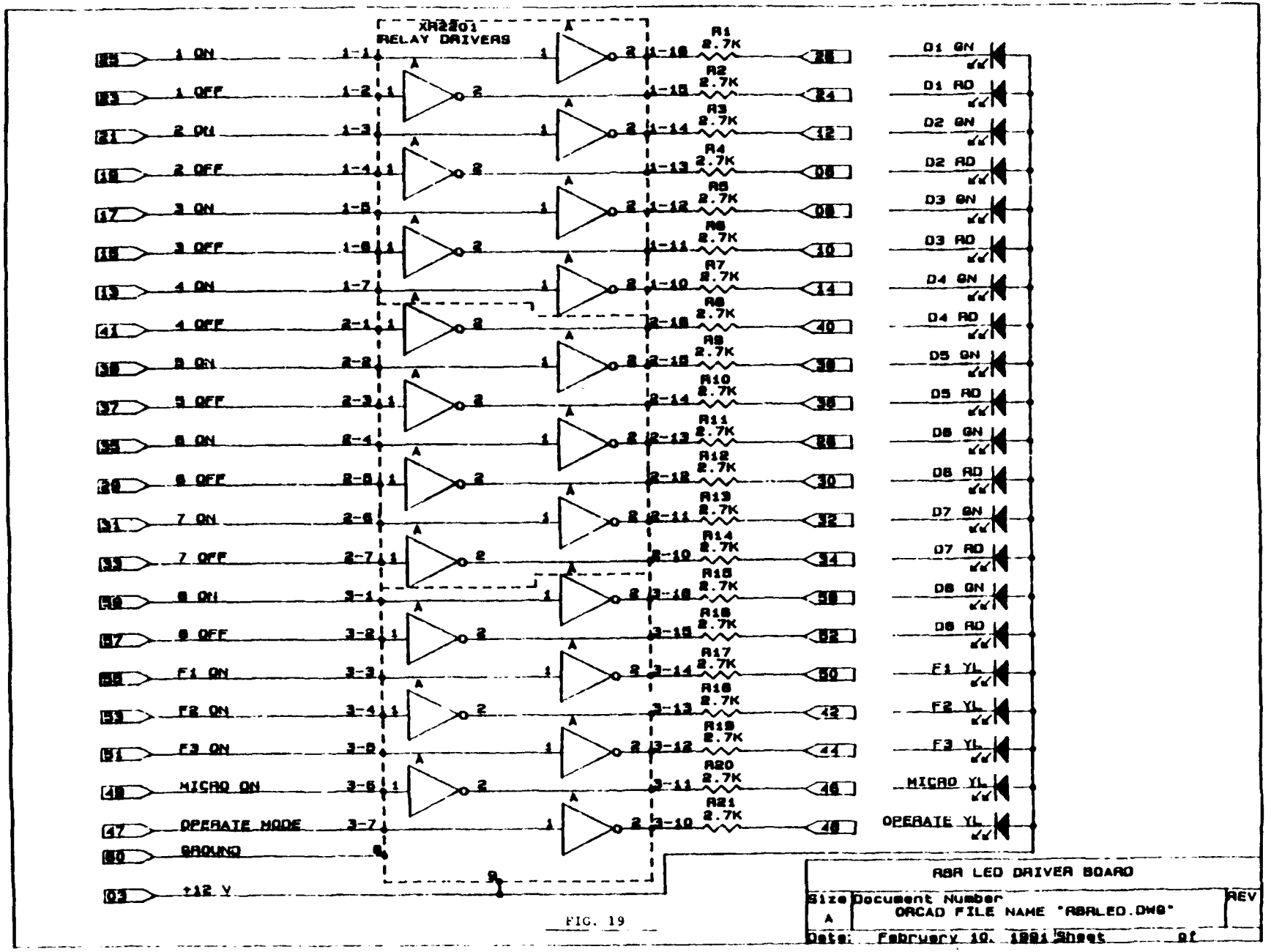
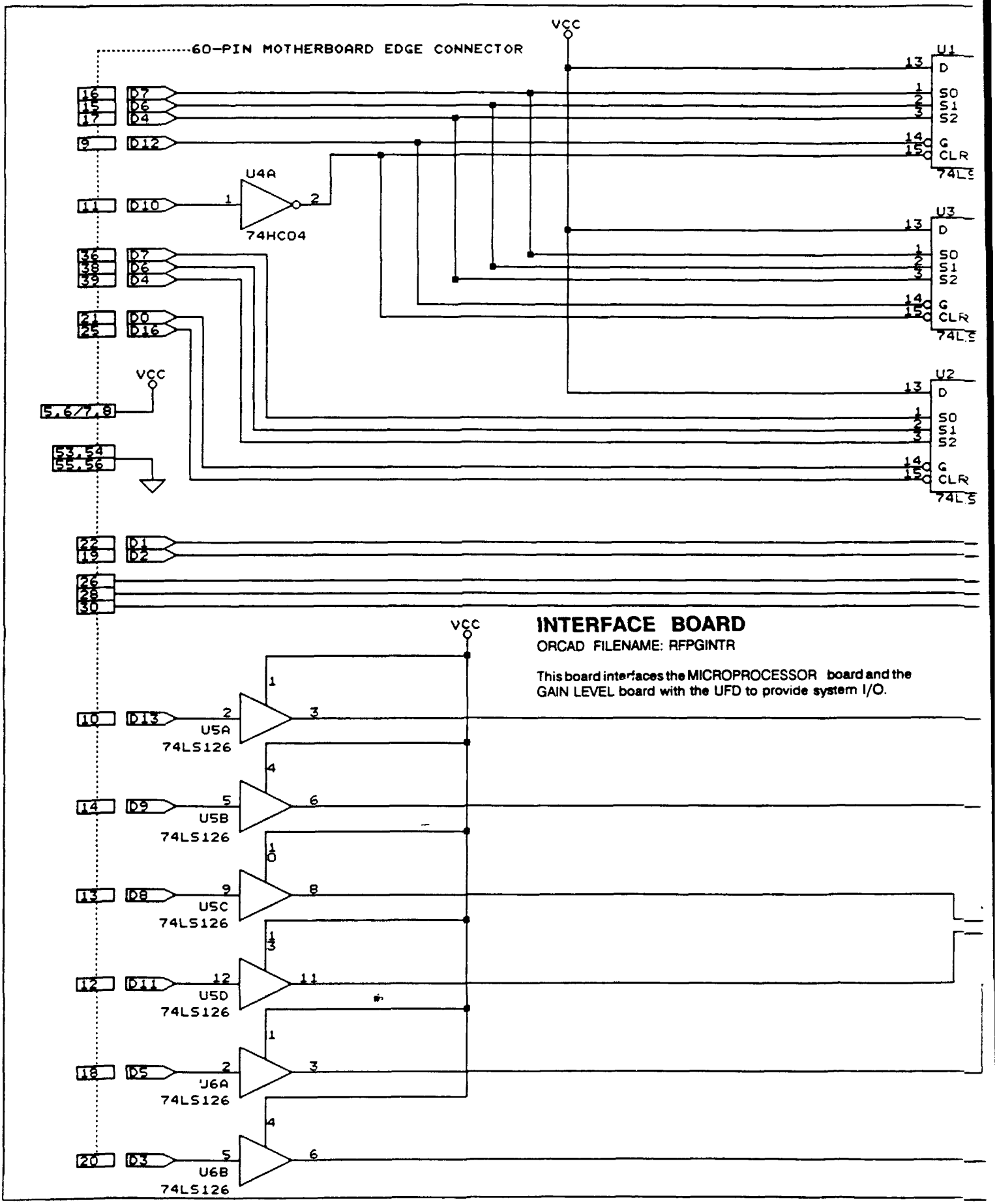

XH2201
RELAY DRIVERS
1 ON
1 OFF
2 ON
2 OFF
3 ON
3 OFF
4 ON
4 OFF
5 ON
5 OFF
6 ON
6 OFF
7 ON
7 OFF
8 ON
8 OFF
F1 ON
F2 ON
F3 ON
MICRO ON
OPERATE MODE
GROUND
+12 V
R1 2.7K
R2 2.7K
R3 2.7K
R4 2.7K
R5 2.7K
R6 2.7K
R7 2.7K
R8 2.7K
R9 2.7K
R10 2.7K
R11 2.7K
R12 2.7K
R13 2.7K
R14 2.7K
R15 2.7K
R16 2.7K
R17 2.7K
R18 2.7K
R19 2.7K
R20 2.7K
R21 2.7K
D1 GN
D1 RD
D2 GN
D2 RD
D3 GN
D3 RD
D4 GN
D4 RD
D5 GN
D5 RD
D6 GN
D6 RD
D7 GN
D7 RD
D8 GN
D8 RD
F1 YL
F2 YL
F3 YL
MICRO YL
OPERATE YL
RBR LED DRIVER BOARD
Size A
Document Number
ORCAD FILE NAME "RBRLED.DWG"
REV
Date: February 10, 1991 Sheet of

FIG. 19



INTERFACE BOARD

ORCAD FILENAME: RFPGINTR

This board interfaces the MICROPROCESSOR board and the GAIN LEVEL board with the UFD to provide system I/O.

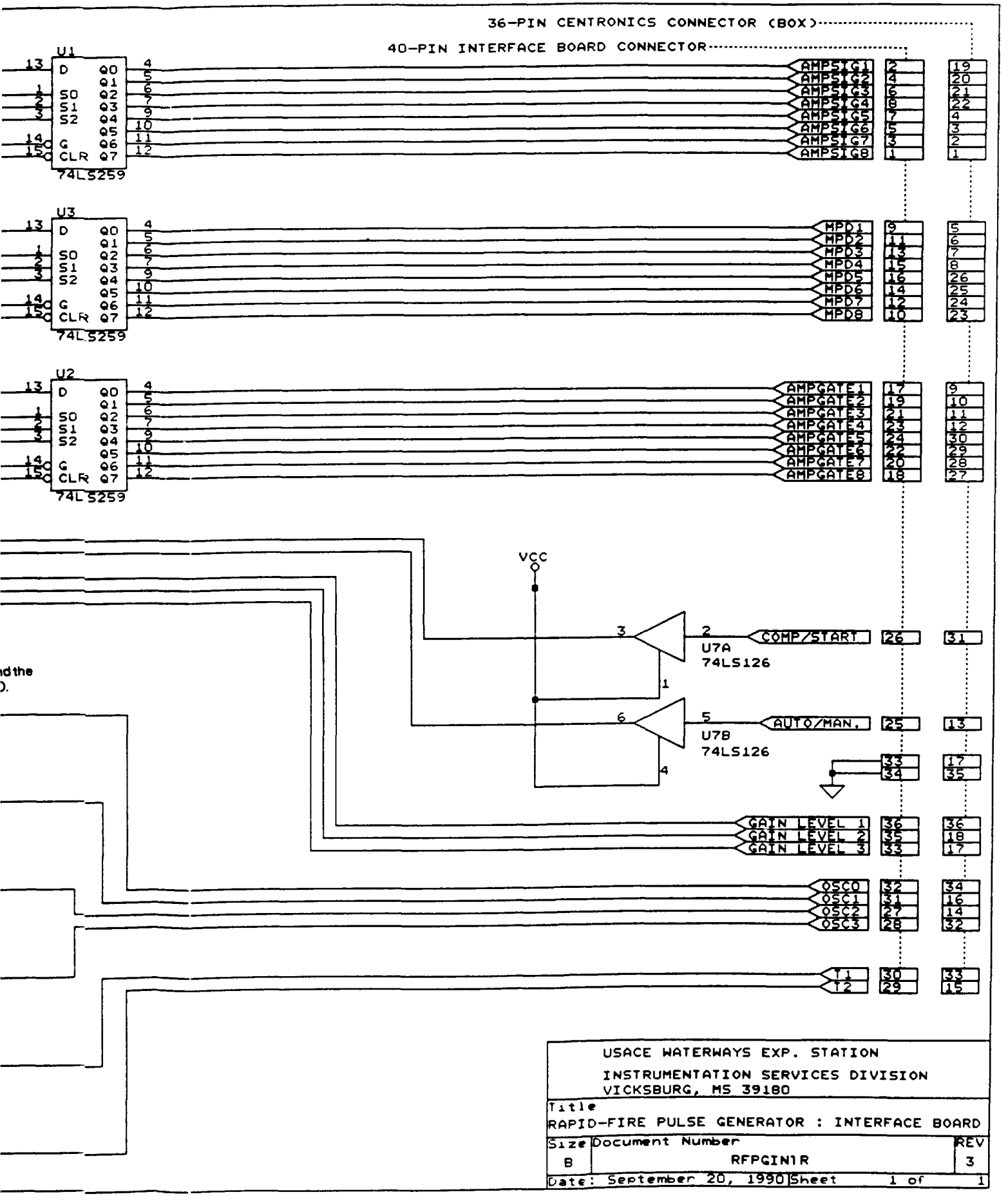
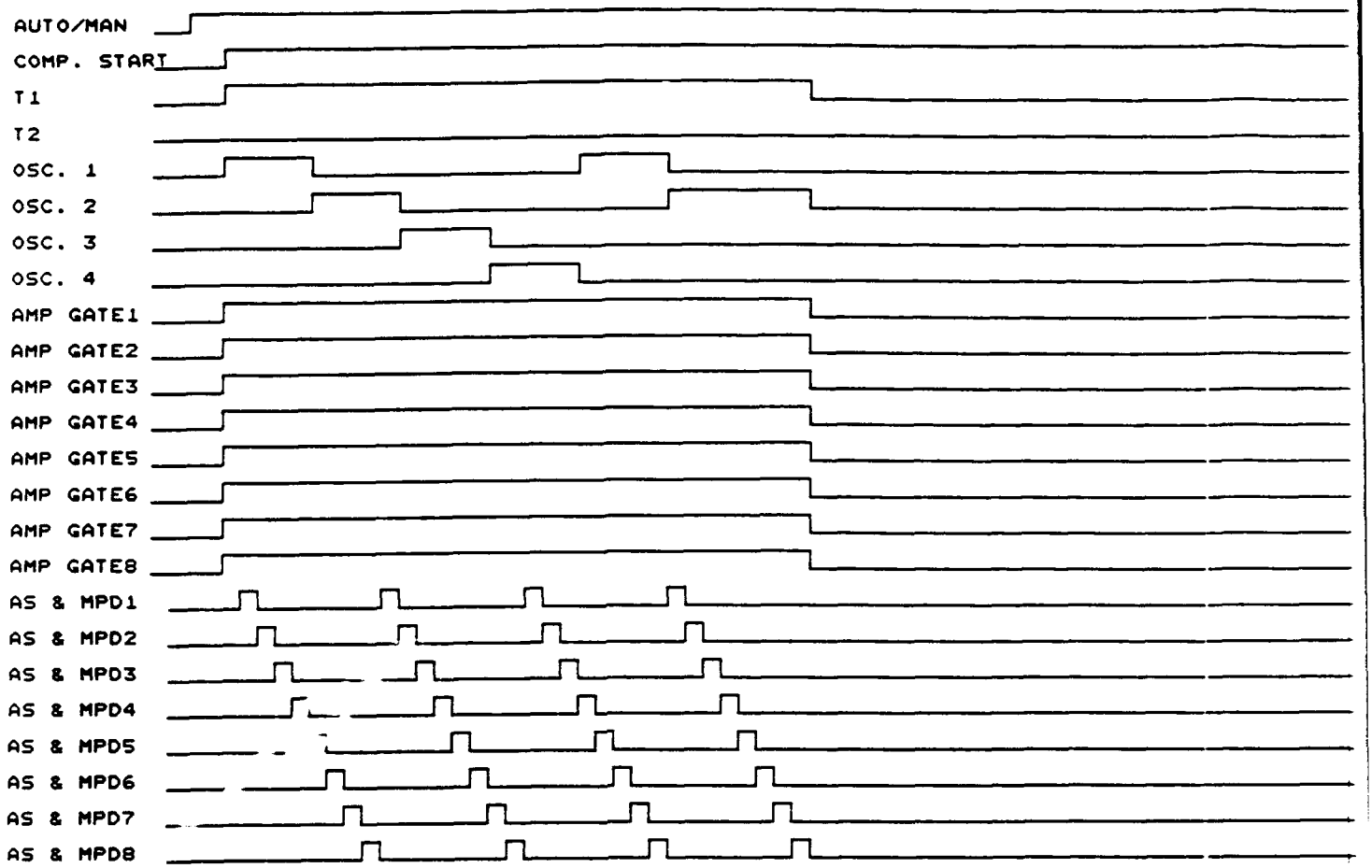
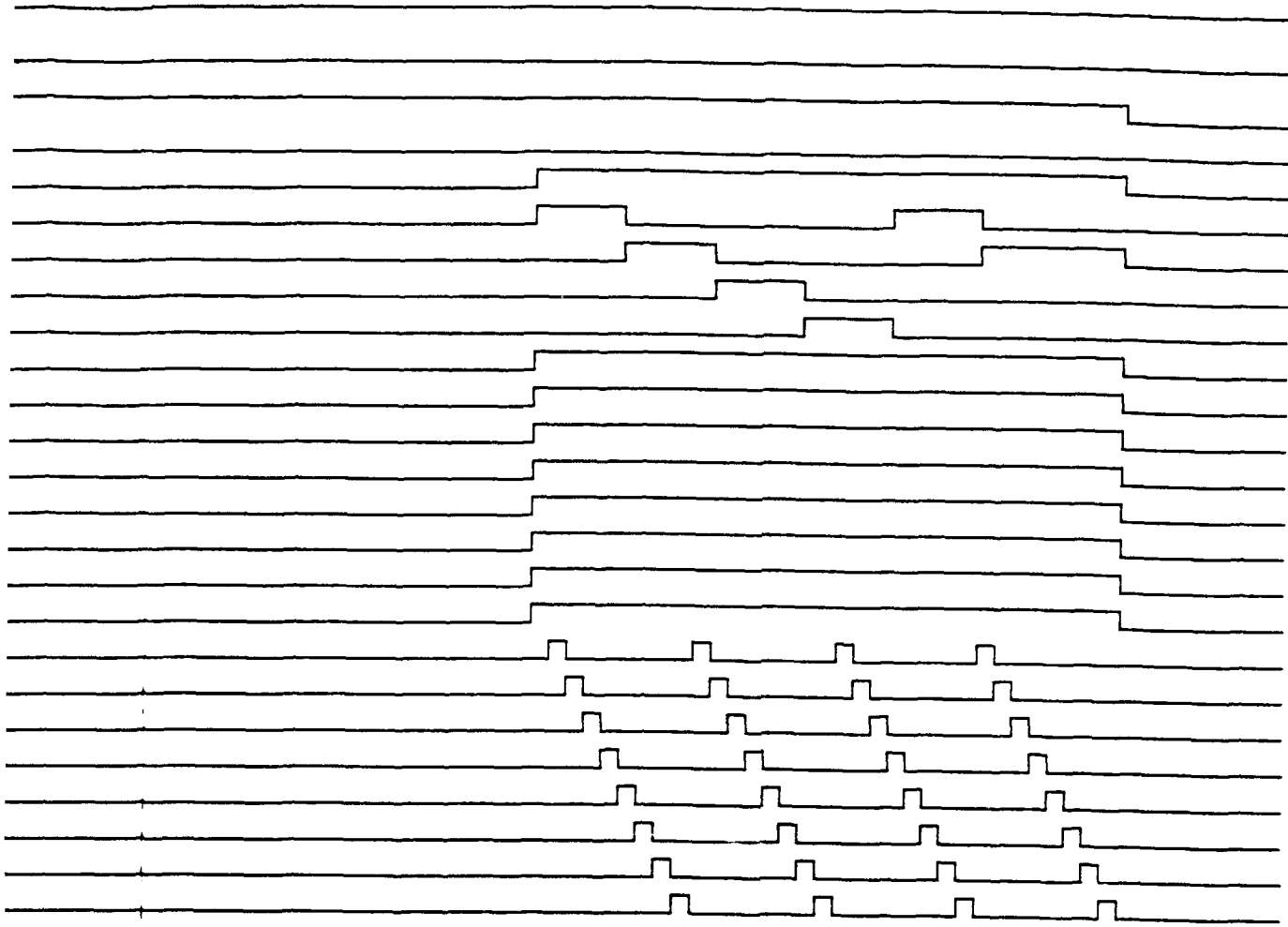

36-PIN CENTRONICS CONNECTOR (BOX)
40-PIN INTERFACE BOARD CONNECTOR
U1
U3
U2
74LS259
VCC
U7A
74LS126
U7B
74LS126
COMP/START
AUTO/MAN.
GAIN LEVEL 1
GAIN LEVEL 2
GAIN LEVEL 3
OSC0
OSC1
OSC2
OSC3
T1
T2
USACE WATERWAYS EXP. STATION
INSTRUMENTATION SERVICES DIVISION
VICKSBURG, MS 39180
Title
RAPID-FIRE PULSE GENERATOR : INTERFACE BOARD
Size
B
Document Number
RFPGIN1R
REV
3
Date: September 20, 1990
Sheet 1 of 1

FIG. 20



T1	USER DEFINED TIME. LIMITS ARE FROM 10 MINUTES TO 60 MINUTES.
T2	USER DEFINED TIME. LIMITS ARE FROM 1 MINUTE TO 30 MINUTES.
TIME BETWEEN T1 AND T2	USER DEFINED TIME. LIMITS ARE FROM 10 MINUTES TO 60 MINUTES.
OSC. 1 – OSC. 4	USER DEFINED TIME. LIMITS ARE FROM 5 MINUTES TO 15 MINUTES. FIRING ORDER IS ALSO USER DEFINED : NOT NECESSARILY OSC 1, OSC 2, O
AMP GATE1 – AMP GATE8	CONTINUOUSLY ENABLED WHENEVER T1 OR T2 IS HIGH.
AS & MPD1 – AS & MPD8	AS & MPD REFER TO AMP SIGNAL AND MISSING PULSE DECTECTOR RESPECTIVE PULSES ARE FIRED CONTINUOUSLY WHENEVER T1 OR T2 IS HIGH. FIRING STARTS APPROXIMATELY 10 MS AFTER AMP GATES ARE ENABLED. PULSES ARE 200 MS APART : THAT IS, EACH CHANNEL PRODUCES 5 PULSES / PULSE WIDTH PROGRESSES AS FOLLOWS: 7 MS FOR 15 SECONDS 10 MS FOR 15 SECONDS 15 MS FOR THE REMAINDER OF THE ACTIVE MODE (T1 OR T2).

FIG. 21



* NOTE, AFTER PREDETERMINED VALUES HAVE BEEN ENTERED IN THE AUTOMATIC MODE,
THE RFPG WILL BEGIN EXECUTION AFTER THE COMPUTER START LINE GOES HIGH
OR IF AN <S> KEY IS PRESSED.
THE RFPG WILL STOP EXECUTION AFTER THE COMPUTER START LINE GOES LOW
OR IF A <Q> KEY IS PRESSED.

ES.

.

ES.

5.
, OSC 2, OSC 3, OSC 4.

RESPECTIVELY.

BLED.
5 PULSES / SECOND.

2).

USACE WATERWAYS EXP. STATION INSTRUMENTAION SERVICES DIVISION VICKSBURG, MS 39180		
Title RAPID-FIRE PULSE GENERATOR : TIMING DIAGRAM		
Size B	Document Number RFPGTIM	RE 1
Date: February 28, 1990	Sheet 1 of	

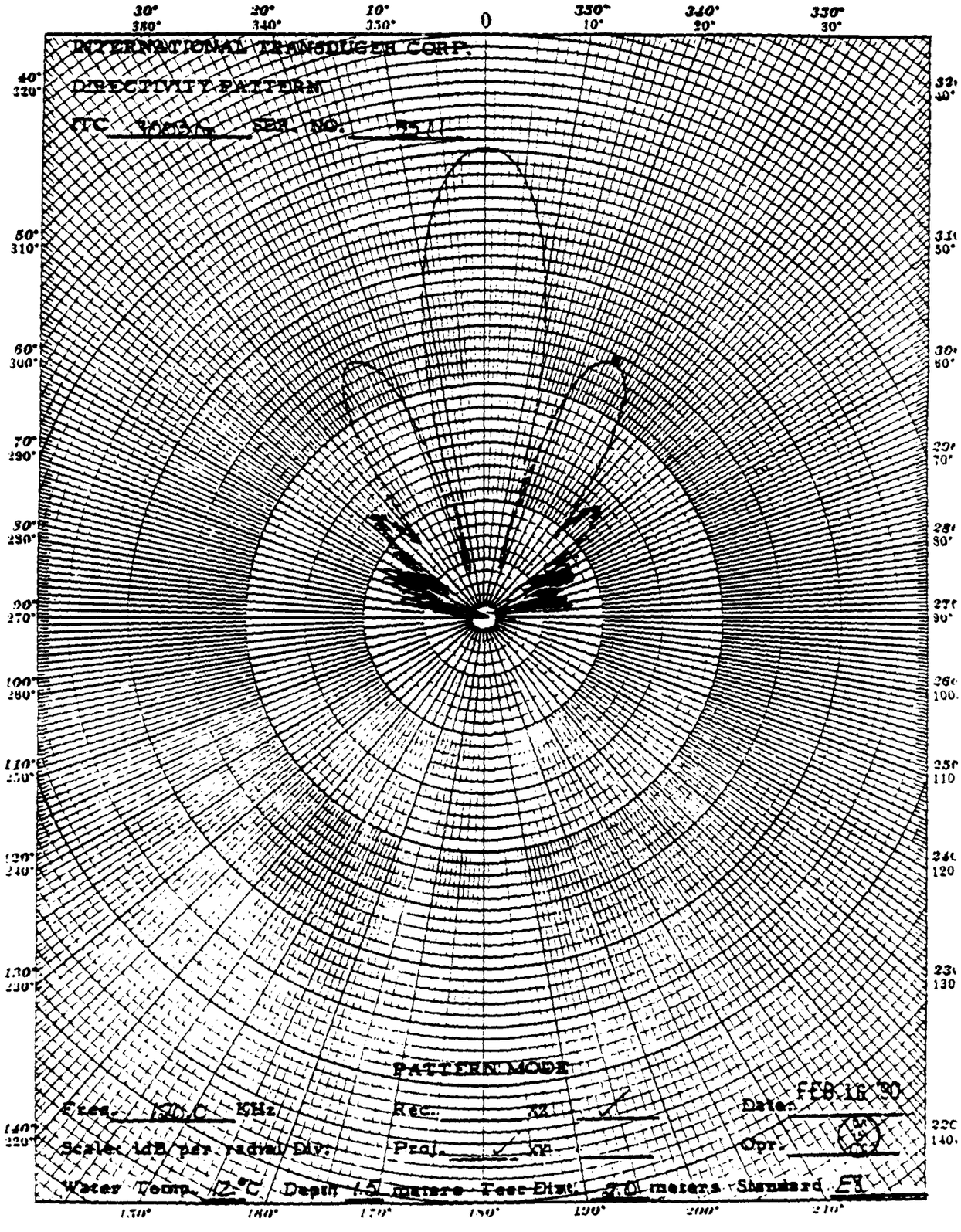

INTERNATIONAL TRANSDUCER CORP.
DIRECTIVITY PATTERN
ITC 3003/S SER. NO. 351
PATTERN MODE
Fres. 120/C KHz
Rec. XX
Proj. XX
Date: FEB 16 '80
Opr.
Scale: dB per radial DIV.
Water Temp. 12°C Depth 15 meters Test Dist. 9.0 meters Standard ES

FIG. 22

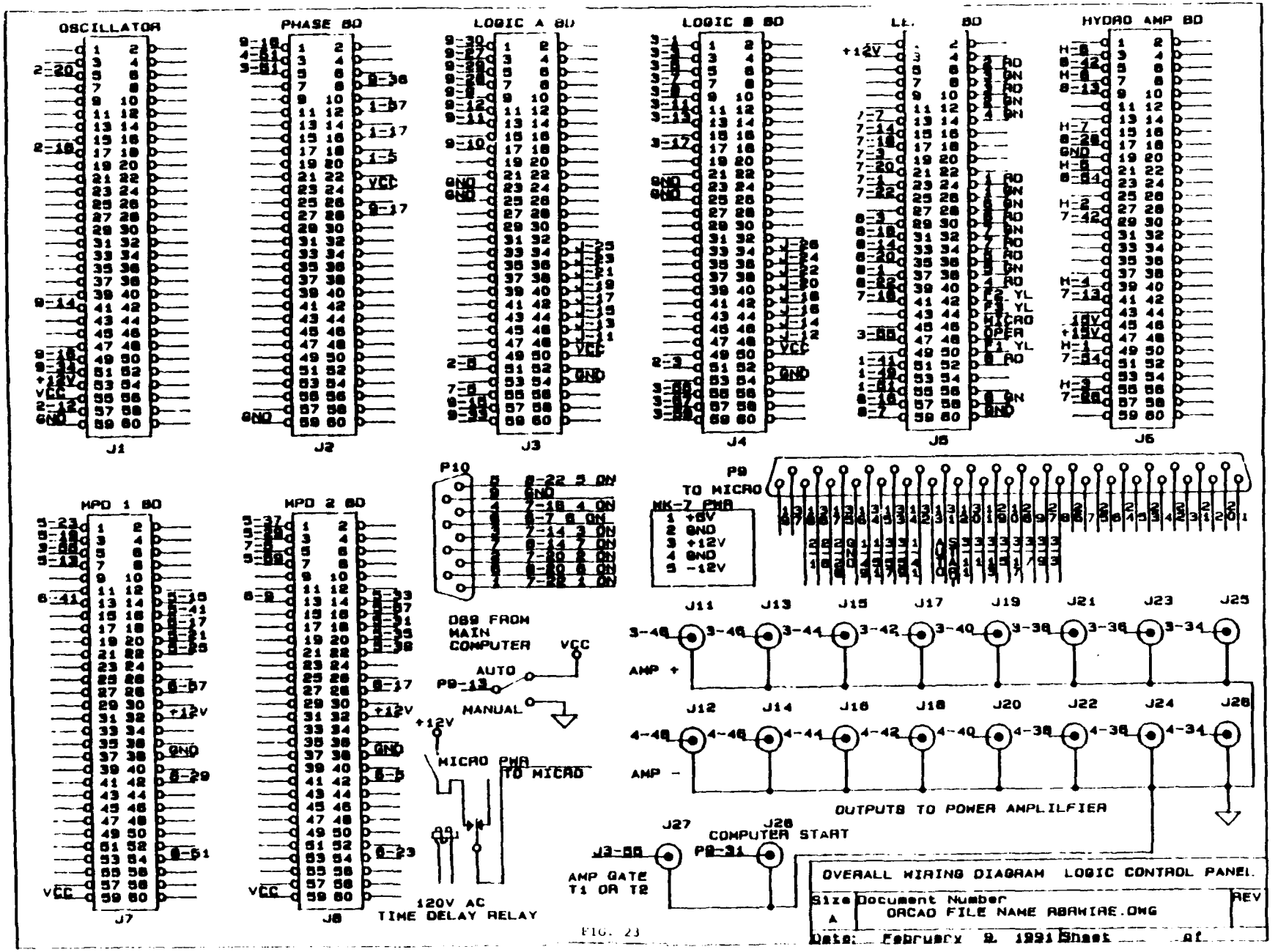

OSCILLATOR
PHASE BD
LOGIC A BD
LOGIC B BD
LL. BD
HYDRO AMP BD
J1
J2
J3
J4
J5
J6
MPD 1 BD
MPD 2 BD
J7
J8
P10
DB9 FROM MAIN COMPUTER
P9
TO MICRO
MK-7 PWR
1 +8V
2 GND
3 +12V
4 GND
5 -12V
AUTO
P9-13
MANUAL
VCC
+12V
MICRO PWR
TO MICRO
120V AC
TIME DELAY RELAY
J11
J13
J15
J17
J19
J21
J23
J25
AMP +
J12
J14
J16
J18
J20
J22
J24
J26
AMP -
OUTPUTS TO POWER AMPLILFIER
J27
J28
COMPUTER START
J3-50
P9-31
AMP GATE
T1 OR T2
OVERALL WIRING DIAGRAM LOGIC CONTROL PANEL
Size
A
Document Number
ORCAD FILE NAME ABWIRE.DWG
REV
Date: February 9, 1991
Sheet
of

FIG. 23

Table 1

RAPID FIRE PULSE GENERATOR (RFPG) SYSTEM INPUT/OUTPUT

36-Pin Centronics Connector	40-Pin Interface Board Connector	Fucntion
1	1	AMP. SIGNAL 8
19	2	AMP. SIGNAL 1
2	3	AMP. SIGNAL 7
20	4	AMP. SIGNAL 2
3	5	AMP. SIGNAL 6
21	6	AMP. SIGNAL 3
4	7	AMP. SIGNAL 5
22	8	AMP. SIGNAL 4
5	9	MPD 1
23	10	MPD 8
6	11	MPD 2
24	12	MPD 7
7	13	MPD 3
25	14	MPD 6
8	15	MPD 4
26	16	MPD 5
9	17	AMP. GATE 1
27	18	AMP. GATE 8
10	19	AMP. GATE 2
28	20	AMP. GATE 7
11	21	AMP. GATE 3
29	22	AMP. GATE 6
12	23	AMP. GATE 4
30	24	AMP. GATE 5
13	25	AUTO/MAN MODE (INPUT)
31	26	MICRO START/STOP (INPUT)
14	27	OSCILLATOR 3
32	28	OSCILLATOR 4 (Do not use)
15	29	T2
33	30	T1
16	31	OSCILLATOR 2
34	32	OSCILLATOR 1
17	33	GAIN LEVEL 3
35	34	GND
18	35	GAIN LEVEL 2
36	36	GAIN LEVEL 1

* All signals are outputs unless stated otherwise in function description.

Table 2

MICROPROCESSOR BOARD

This listing was compiled as an alternative to drawing a schematic of the specified board. This was done since the only components on the board are the two Tattle V's, three sips of pulldown resistors, and two UART connectors.

Corresponding sMARTWORK FILE for PRINTED CIRCUIT BOARD — TAT5FIR

ORIGIN			DESTINATION		
MICRO I	Pin 14	-STBY	MICRO I	Pin 15	REG 5V
MICRO I	Pin 15	REG 5V	MICRO I	Pin 14	-STBY
MICRO I	Pin 16	I/O D16	EDGE CON.	Pin 25	CLR AMP GATE & MPD
MICRO I	Pin 17	I/O D15	MICRO II	Pin 26	I/O D9
MICRO I	Pin 18	I/O D14	EDGE CON.	Pin 23	GAIN LEVEL CLOCK
MICRO I	Pin 19	I/O D13	EDGE CON.	Pin 10	OSC. SEL 0
MICRO I	Pin 20	DIG.GND	EDGE CON.	Pin 53,55	Mother Board Gnd
MICRO I	Pin 21	I/O D12	MICRO II	Pin 22	I/O D11
MICRO I	Pin 22	I/O D11	EDGE CON.	Pin 12	OSC. SEL 3
MICRO I	Pin 23	UDI	MICRO I UART CON.	Pin 2	UDI
MICRO I	Pin 24	UDO	MICRO I UART CON.	Pin 6	UDO
MICRO I	Pin 25	I/O D10	MICRO II	Pin 19	I/O D13
MICRO I	Pin 26	I/O D9	EDGE CON.	Pin 14	OSC. SEL 1
MICRO I	Pin 27	I/O D8	EDGE CON.	Pin 13	OSC. SEL 2
MICRO I	Pin 28	I/O D7	EDGE CON.	Pin 36	ADDR (SEL A) AMP GATE
MICRO I	Pin 29	I/O D6	EDGE CON.	Pin 38	ADDR (SEL B) AMP GATE
MICRO I	Pin 30	I/O D5	EDGE CON.	Pin 18	T1
MICRO I	Pin 31	I/O D4	EDGE CON.	Pin 39	ADDR (SEL C) AMP GATE
MICRO I	Pin 32	I/O D3	EDGE CON.	Pin 20	T2
MICRO I	Pin 33	I/O D2	EDGE CON.	Pin 19	Input Auto/Manual Select
MICRO I	Pin 34	I/O D1	EDGE CON.	Pin 22	Input Computer Start Level
MICRO I	Pin 35	I/O D0	EDGE CON.	Pin 20	Latch AMP GATE & MPD
MICRO I	Pin 37	BAT +	EDGE CON.	Pin 41,43	Mother Board +12V
MICRO II	Pin 14	-STBY	MICRO II	Pin 15	REG 5V
MICRO II	Pin 15	REG 5V	MICRO II	Pin 14	-STBY
MICRO II	Pin 19	I/O D13	MICRO I	Pin 25	I/O D10
MICRO II	Pin 20	DIG.GND	EDGE CON.	Pin 53,55	Mother Board Gnd
MICRO II	Pin 21	I/O D12	EDGE CON.	Pin 9	Latch AMP SIGNAL
MICRO II	Pin 22	I/O D11	MICRO I	Pin 21	I/O D12
MICRO II	Pin 23	UDI	MICRO II UART CON.	Pin 2	UDI
MICRO II	Pin 24	UDO	MICRO II UART CON.	Pin 6	UDO
MICRO II	Pin 25	I/O D10	EDGE CON.	Pin 11	CLR AMP SIGNAL
MICRO II	Pin 26	I/O D9	MICRO I	Pin 17	I/O D15
MICRO II	Pin 28	I/O D7	EDGE CON.	Pin 16	ADDR (SEL A) AMP SIGNAL & MPD
MICRO II	Pin 29	I/O D6	EDGE CON.	Pin 15	ADDR (SEL B) AMP SIGNAL & MPD
MICRO II	Pin 31	I/O D4	EDGE CON.	Pin 17	ADDR (SEL C) AMP SIGNAL & MPD
MICRO II	Pin 37	BAT +	EDGE CON.	Pin 41,43	Mother Board +12V
MICRO I UART	Pin 1	GND	EDGE CON.	Pin 53,55	Mother Board Gnd
MICRO I UART	Pin 2	UDI	MICRO I	Pin 23	UDI
MICRO I UART	Pin 4	+ 5V	EDGE CON.	Pin 46,48	Mother Board +5V
MICRO I UART	Pin 6	UDO	MICRO I	Pin 24	UDO
MICRO II UART	Pin 1	GND	EDGE CON.	Pin 53,55	Mother Board Gnd
MICRO II UART	Pin 2	UDI	MICRO II	Pin 23	UDI
MICRO II UART	Pin 4	+ 5V	EDGE CON.	Pin 46,48	Mother Board +5V
MICRO II UART	Pin 6	UDO	MICRO II	Pin 24	UDO

All Digital Output lines of each Micro are tied to a pulldown resistor with the exception of D4. D4, on both MICROs must stay pulled high as it is shipped from the factory.

Table 3

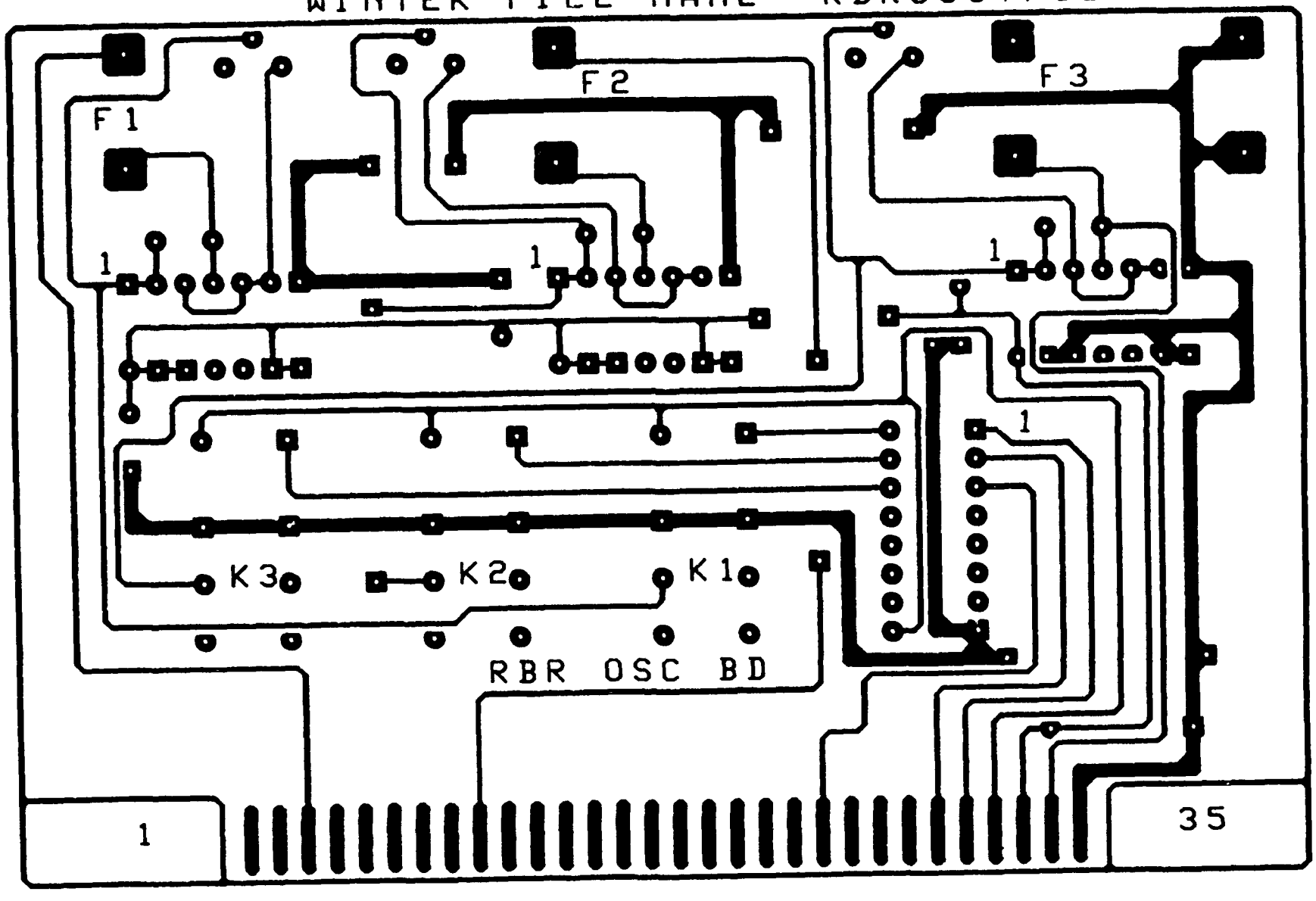
RAPID FIRE PULSE GENERATOR (RFPG)
MOTHER BOARD CONNECTOR PINOUT

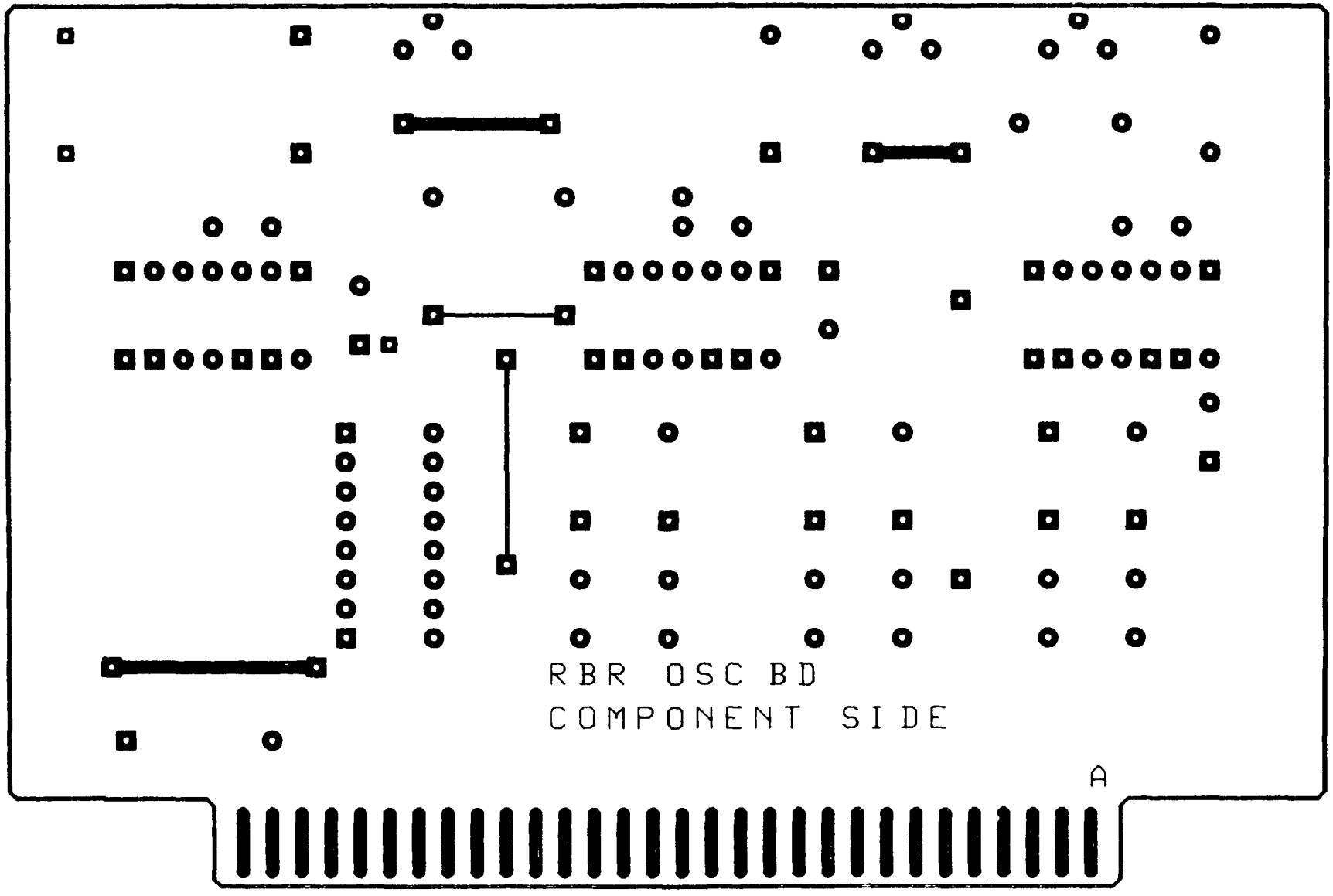
PIN NO.	DATA	PIN NO.	DATA
1	COMMON	2	COMMON
3	COMMON	4	COMMON
5	+5 VDC	6	+5 VDC
7	+5 VDC	8	+5 VDC
9	D12 MICRO II (LATCH AMP SIG & MPD)	10	D13 MICRO I (OSC 0)
11	D10 MICRO II (CLEAR AMP SIG & MPD)	12	D11 MICRO I (OSC 3)
13	D8 MICRO I (OSC 2)	14	D9 MICRO I (OSC 1)
15	D6 MICRO II (S1 ADDR SEL)	16	D7 MICRO II (S0 ADDR SEL)
17	D4 MICRO II (S2 ADDR SEL)	18	D5 MICRO I (T1)
19	D2 MICRO I (AUTO/MAN SEL)	20	D3 MICRO I (T2)
21	D0 MICRO I (LATCH AMP GATE)	22	D1 MICRO I (COMPUTER START/STOP)
23	D14 MICRO I (GAIN LEVEL CLK)	24	D15 MICRO I (HOUSEKEEPING)
25	D16 MICRO I (CLEAR AMP GATE)	26	GAIN LEVEL 1
27	NO CONNECTION	28	GAIN LEVEL 2
29	NO CONNECTION	30	GAIN LEVEL 3
31	NO CONNECTION	32	NO CONNECTION
33	NO CONNECTION	34	NO CONNECTION
35	NO CONNECTION	36	D7 MICRO I (S0 ADDR SEL)
37	NO CONNECTION	38	D6 MICRO I (S1 ADDR SEL)
39	NO CONNECTION	40	NO CONNECTION
41	+12 VDC UNREGULATED	42	+12 VDC UNREGULATED
43	+12 VDC UNREGULATED	44	+12 VDC UNREGULATED
45	+5 VDC	46	+5 VDC
47	+5 VDC	48	+5 VDC
49	-12 VDC	50	-12 VDC
51	-12 VDC	52	-12 VDC
53	COMMON	54	COMMON
55	COMMON	56	COMMON
57	+12 VDC	58	+12 VDC
59	+12 VDC	60	+12 VDC

Circuit Boards

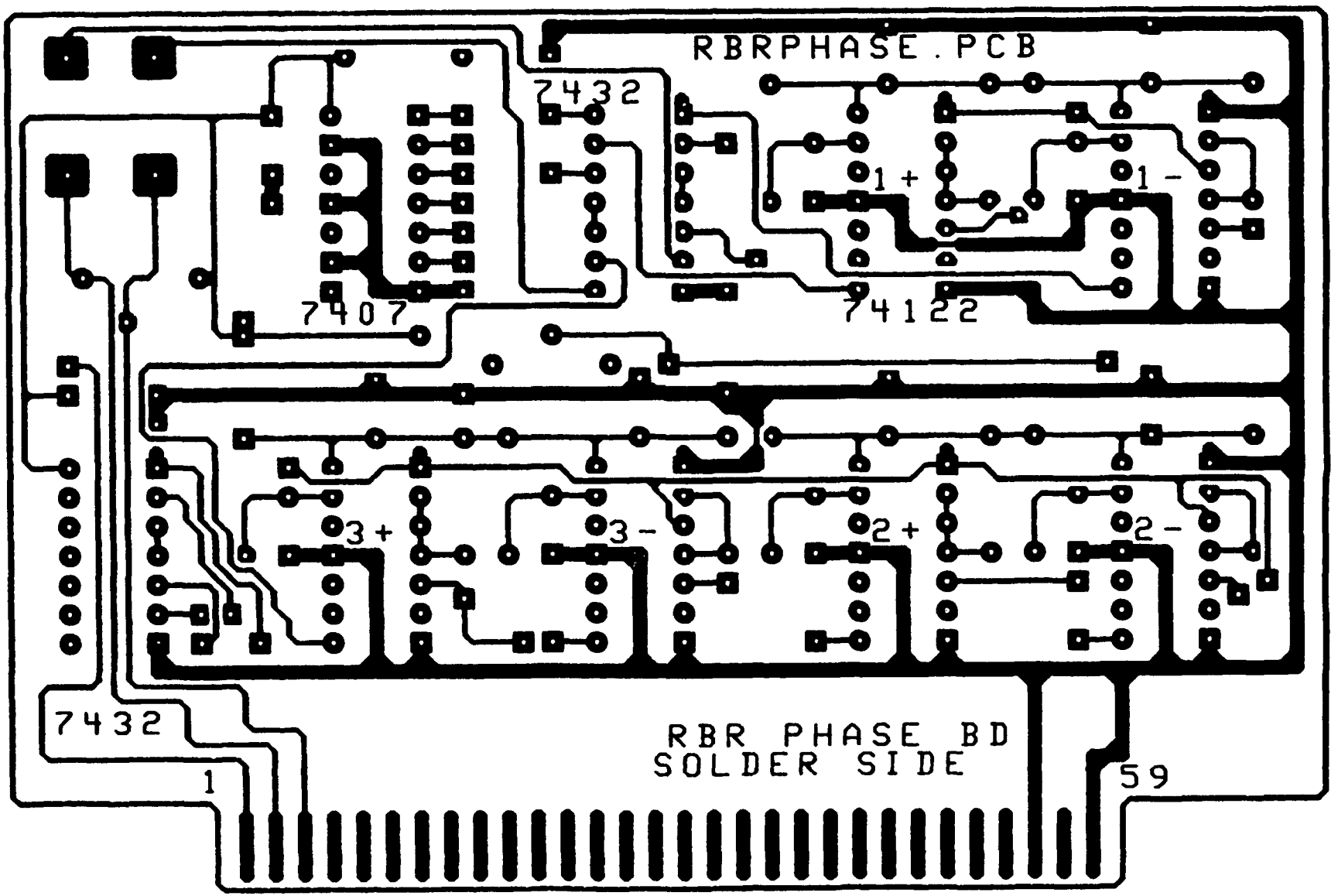
MASTER OSCILLATOR BD

WINTEK FILE NAME "RBROSC.PCB"

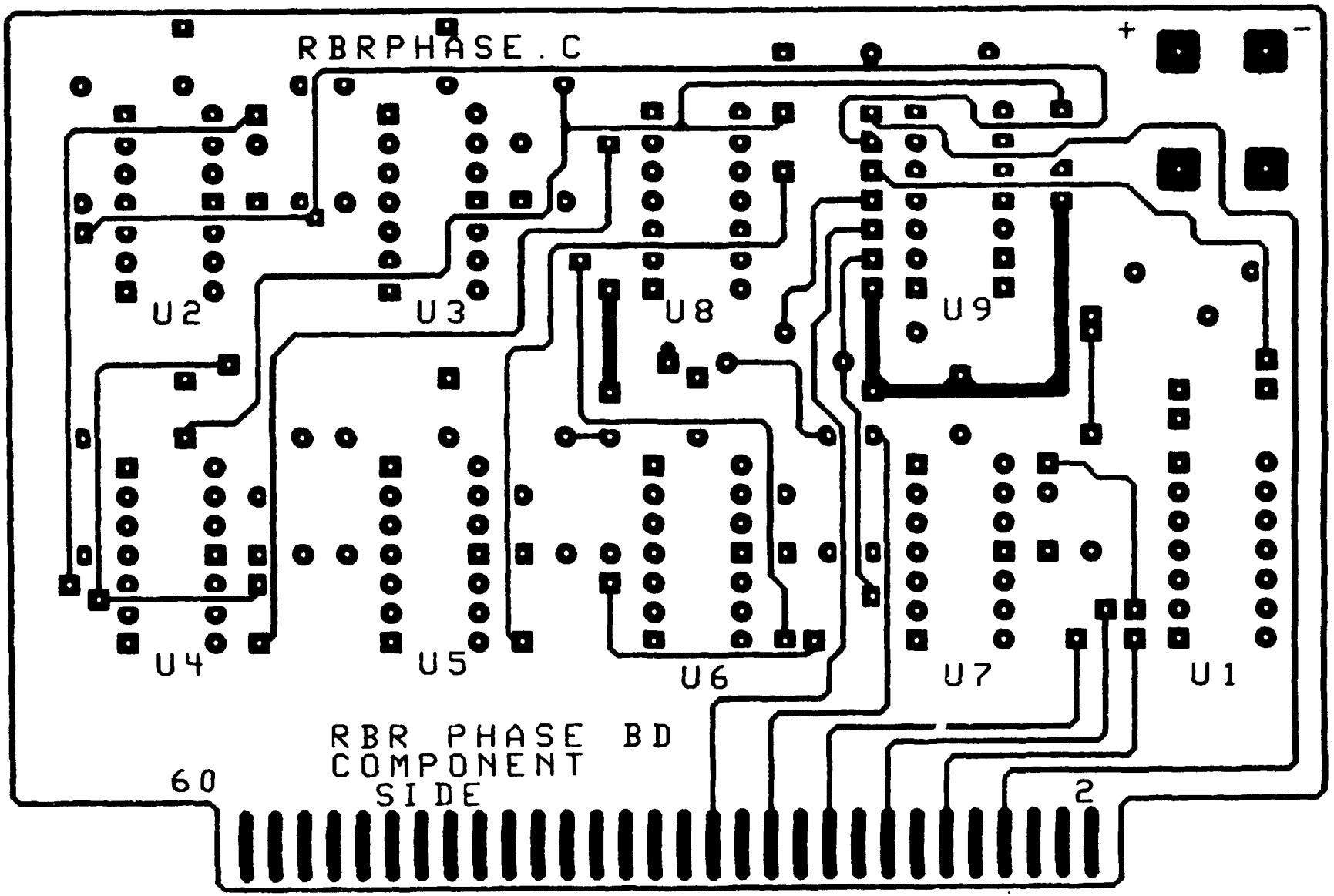



RBR OSC BD
COMPONENT SIDE
A

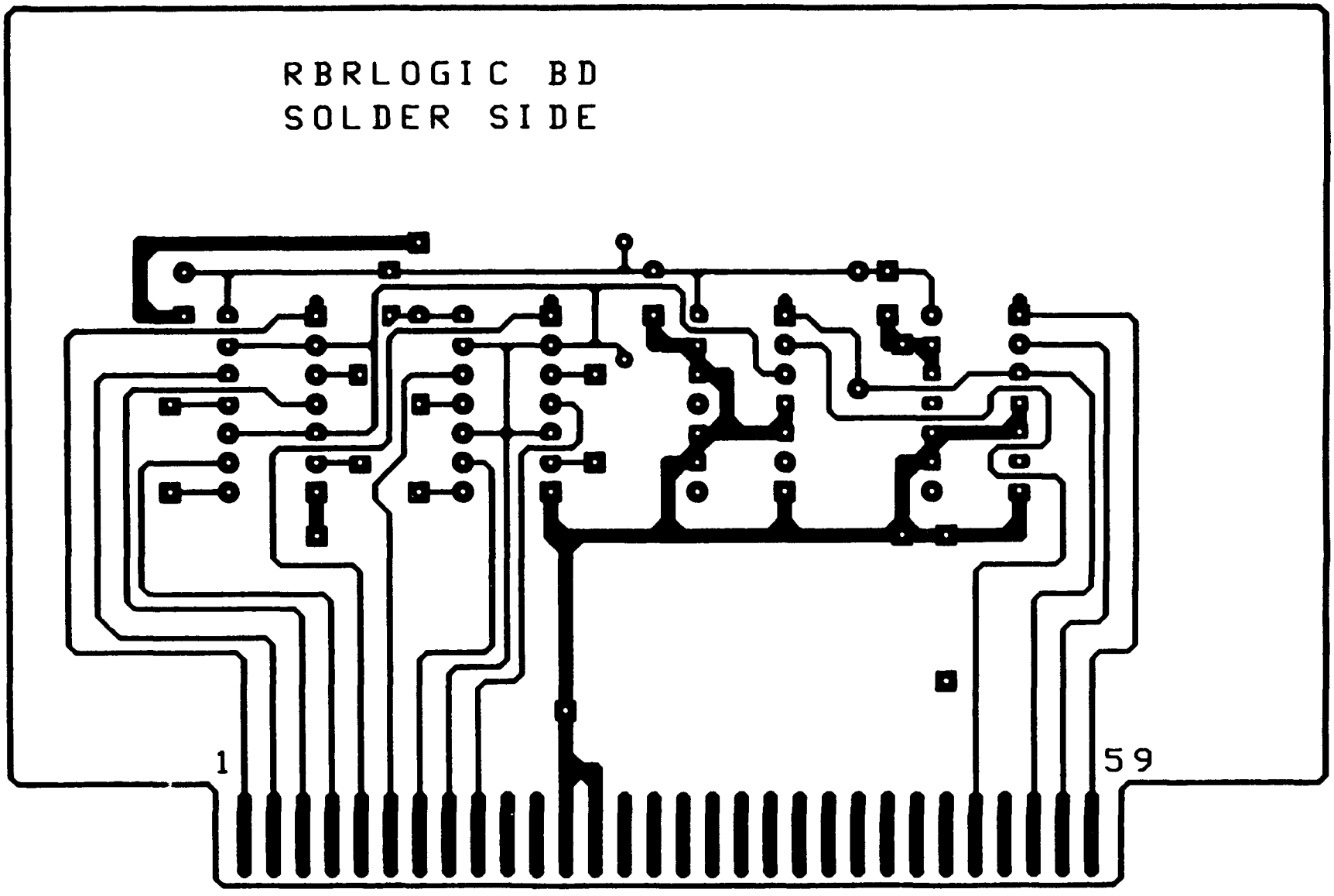
RBR SLOW GAIN BOARD
WINTEK FILE NAME "RBRPHASE.PCB



RBR SLOW GAIN BOARD
WINTEK FILE NAME RBRPHASE . . C



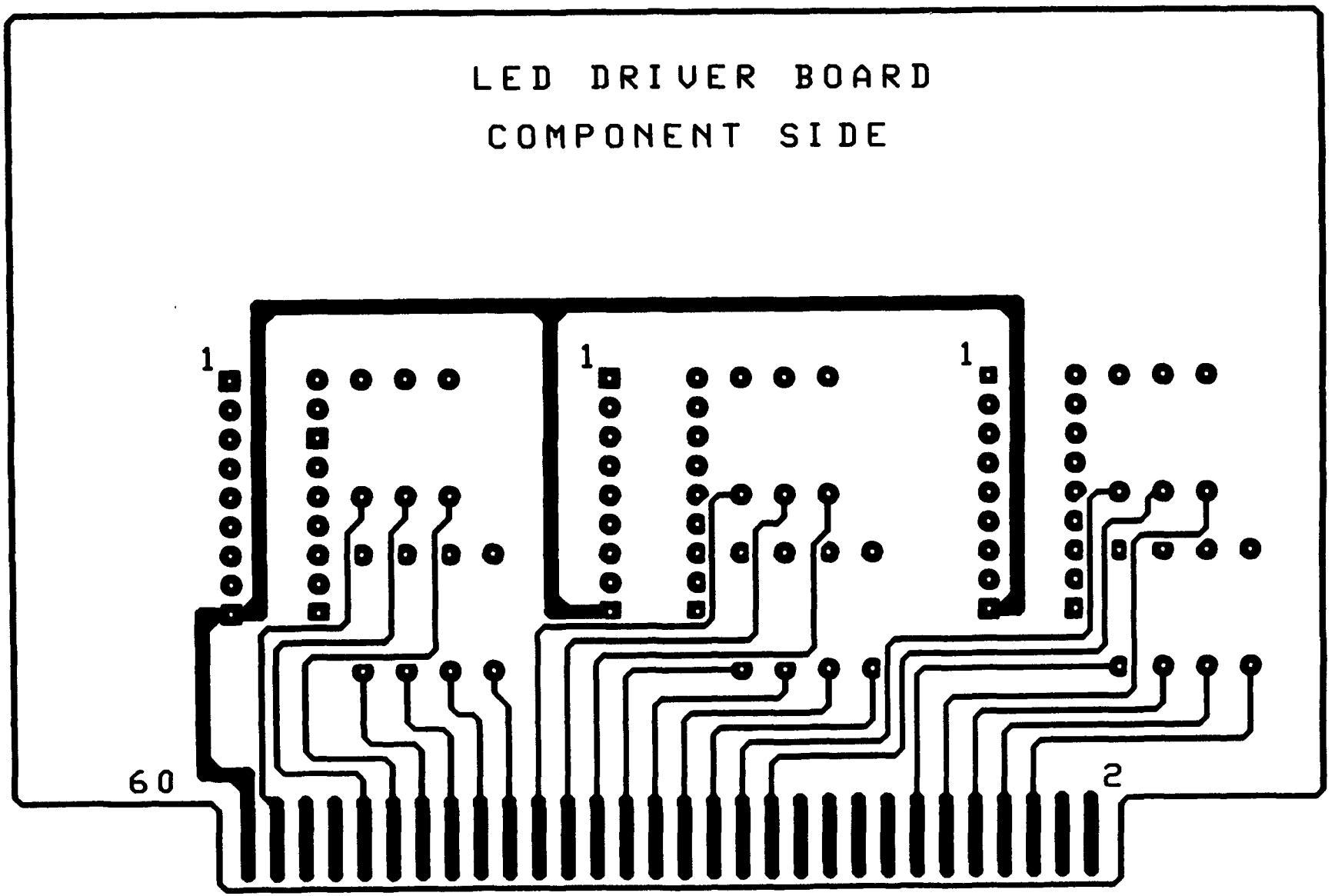
RBRLOGIC BD
SOLDER SIDE



WINTEK FILE NAME "RBRLED.C"

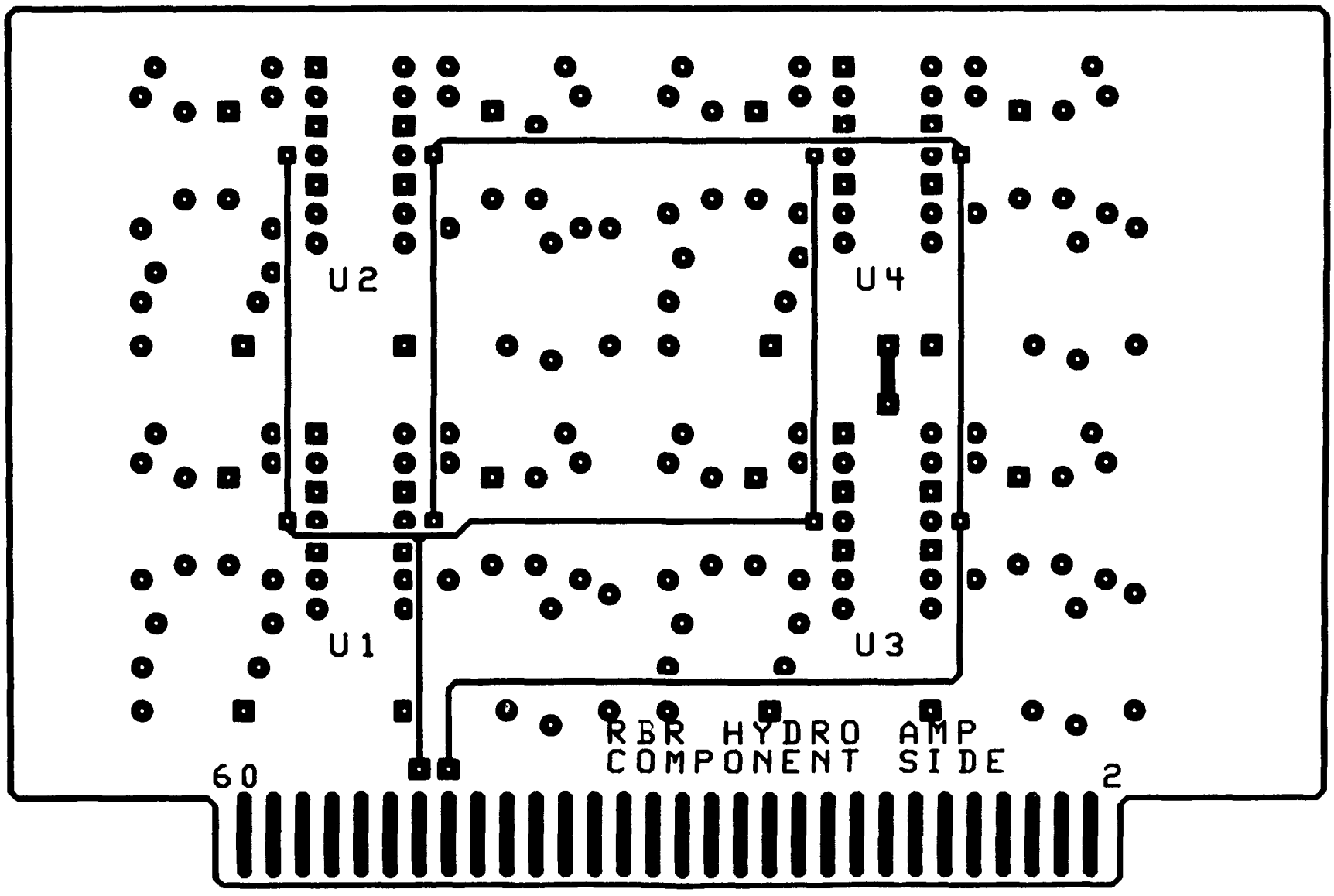
LED DRIVER BOARD

COMPONENT SIDE



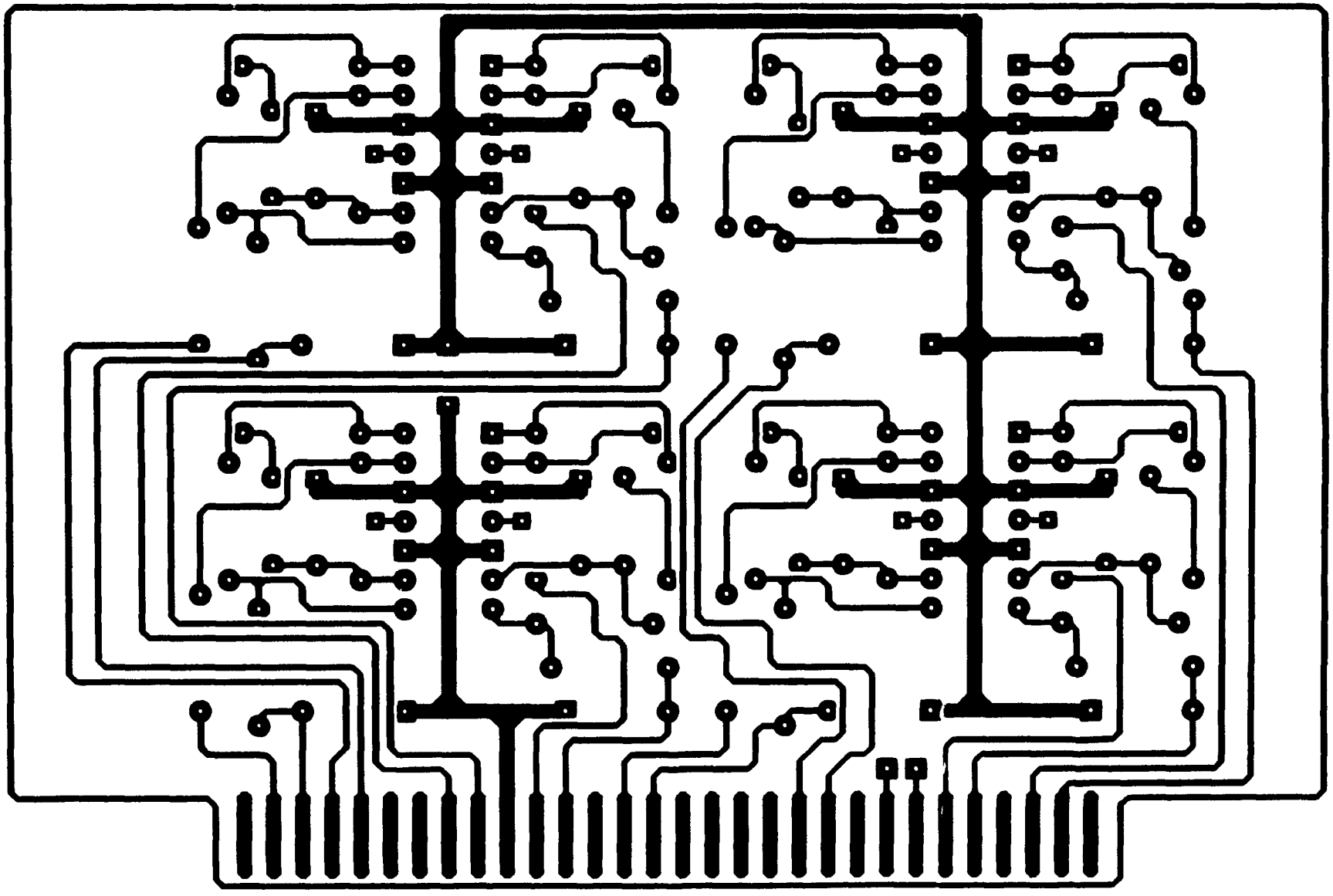
HYDROPHONE AMPLIFIER

WINTEK FILE NAME RBRAMP.C

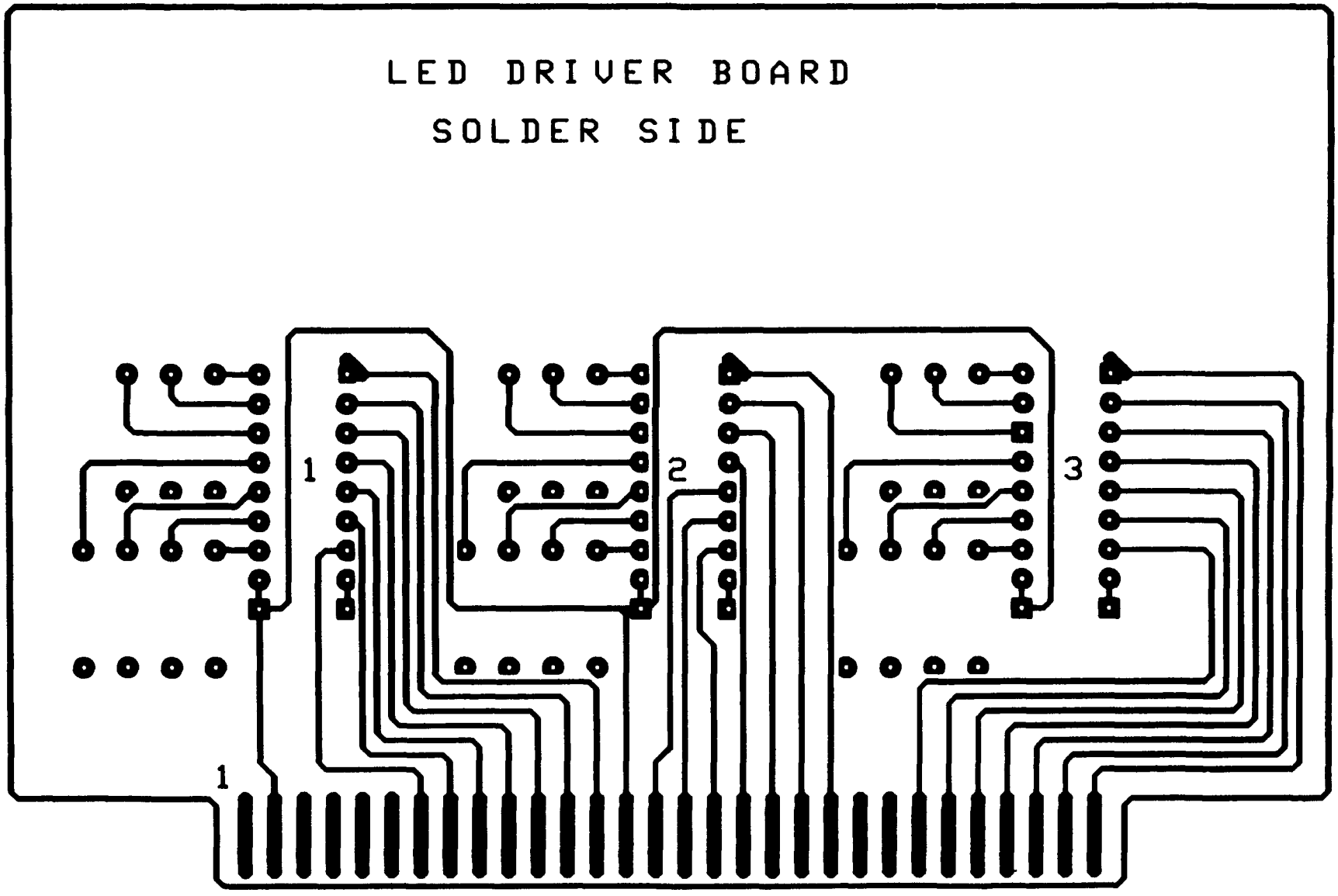


YDROPHONE AMPLIFIER

WINTEK FILE NAME RBRAMP.PCB



WINTEK FILE NAME "RBRLED.PCB"



SSI Gates

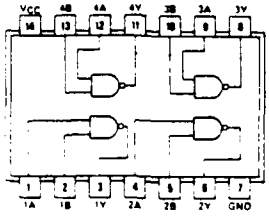
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

00

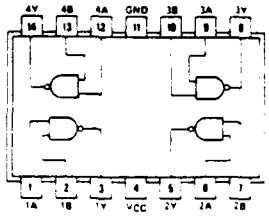
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 86



SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)



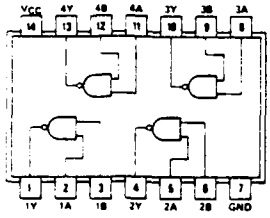
SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

01

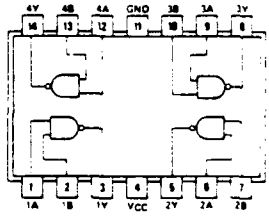
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

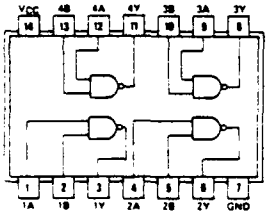
See page 88



SN5401/SN7401(J, N)
SN54LS01/SN74LS01(J, N, W)



SN5401/SN7401(W)
SN54H01/SN74H01(W)
SN54L01/SN74L01(T)



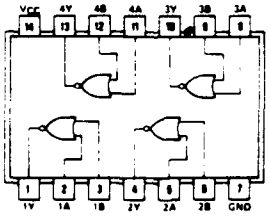
SN54H01/SN74H01(J, N)

02

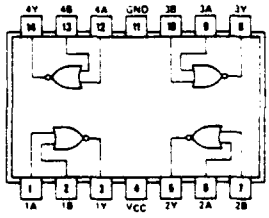
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

See page 92



SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



SN5402/SN7402(W)
SN54L02/SN74L02(T)

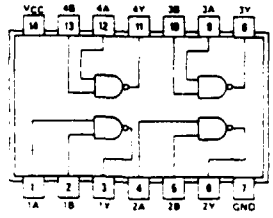
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

03

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

See page 88



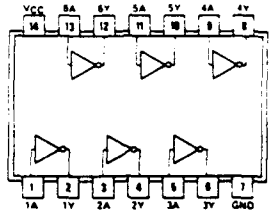
SN5403/SN7403(J, N)
SN54L03/SN74L03(J, N)
SN54LS03/SN74LS03(J, N, W)
SN54S03/SN74S03(J, N, W)

04

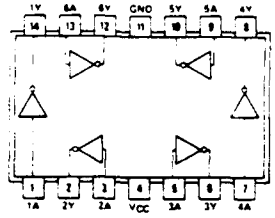
HEX INVERTERS

positive logic:
$Y = \overline{A}$

See page 86



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)



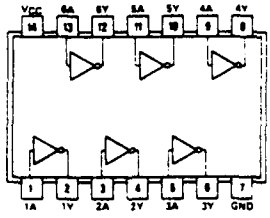
SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

05

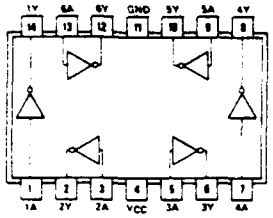
HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A}$

See page 88



SN5405/SN7405(J, N)
SN54H05/SN74H05(J, N)
SN54LS05/SN74LS05(J, N, W)
SN54S05/SN74S05(J, N, W)



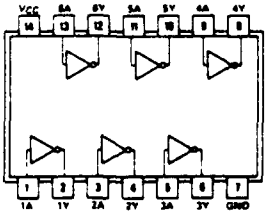
SN5405/SN7405(W)
SN54H05/SN74H05(W)

06

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106



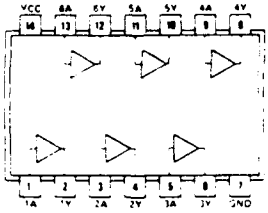
SN5406/SN7406(J, N, W)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

07
HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
Y = A

See page 106

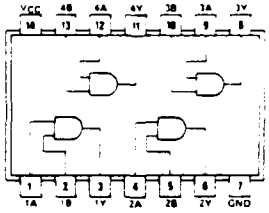


SN5407/SN7407(J, N, W)

08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:
Y = AB

See page 94

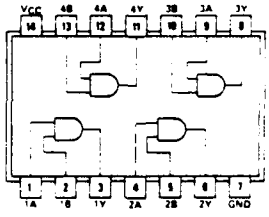


SN5408/SN7408(J, N, W)
SN54LS08/SN74LS08(J, N, W)

09
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
Y = AB

See page 96

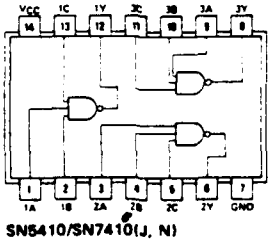


SN5409/SN7409(J, N, W)
SN54LS09/SN74LS09(J, N, W)

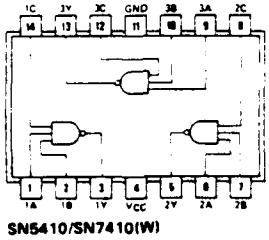
10
TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABC}$

See page 86



SN5410/SN7410(J, N)
SN54H10/SN74H10(J, N)
SN54L10/SN74L10(J, N)
SN54LS10/SN74LS10(J, N, W)
SN54S10/SN74S10(J, N, W)



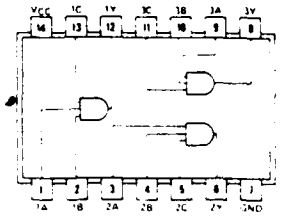
SN5410/SN7410(W)
SN54H10/SN74H10(W)
SN54L10/SN74L10(T)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

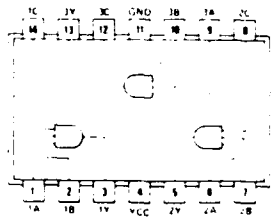
11
TRIPLE 3-INPUT
POSITIVE-AND GATES

positive logic:
$Y = ABC$

See page 94



SN54H11/SN74H11(J, N)
SN54LS11/SN74LS11(J, N, W)
SN54S11/SN74S11(J, N, W)

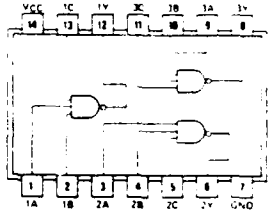


SN54H11/SN74H11(W)

12
TRIPLE 3-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{ABC}$

See page 88

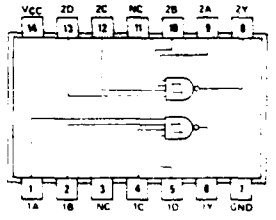


SN5412/SN7412(J, N, W)

13
DUAL 4-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

positive logic:
$Y = \overline{ABCD}$

See page 98



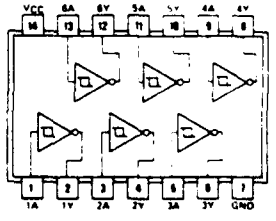
SN5413/SN7413(J, N, W)

NC—No internal connection

14
HEX SCHMITT-TRIGGER
INVERTERS

positive logic:
$Y = \overline{A}$

See page 98



SN5414/SN7414(J, N, W)

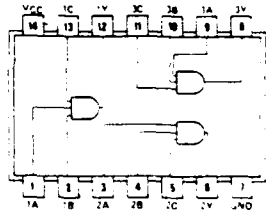
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

15

TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = ABC$

See page 96



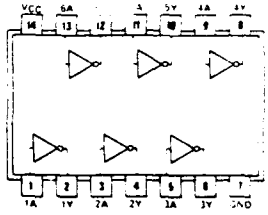
SN54H15/SN74H15(J, N, W)
SN54LS15/SN74LS15(J, N, W)
SN54S15/SN74S15(J, N, W)

16

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106



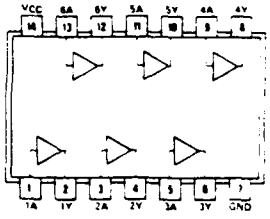
SN5416/SN7416(J, N, W)

17

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = A$

See page 106



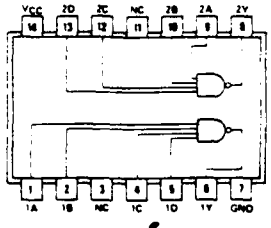
SN5417/SN7417(J, N, W)

20

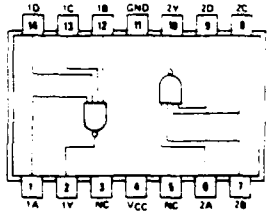
DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$

See page 86



SN5420/SN7420(J, N)
SN54H20/SN74H20(J, N)
SN54L20/SN74L20(J, N)
SN54LS20/SN74LS20(J, N, W)
SN54S20/SN74S20(J, N, W)



SN5420/SN7420(W)
SN54H20/SN74H20(W)
SN54L20/SN74L20(T)

NC—No internal connection

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

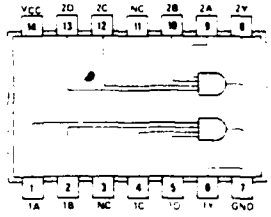
21

DUAL 4-INPUT POSITIVE-AND GATES

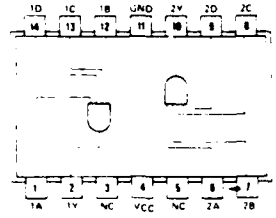
positive logic:

$Y = ABCD$

See page 94



SN54H21/SN74H21(J, N)
SN54LS21/SN74LS21(J, N, W)



SN54H21/SN74H21 (W)

NC—No internal connection

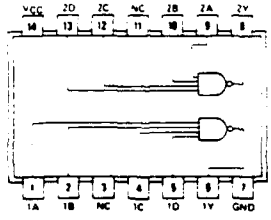
22

DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

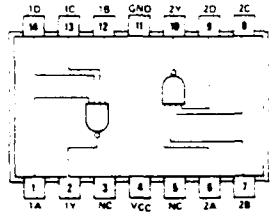
positive logic:

$Y = \overline{ABCD}$

See page 88



SN5422/SN7422(J, N, W)
SN54H22/SN74H22(J, N)
SN54LS22/SN74LS22(J, N, W)
SN54S22/SN74S22(J, N, W)



SN54H22/SN74H22(W)

NC—No internal connection

23

EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

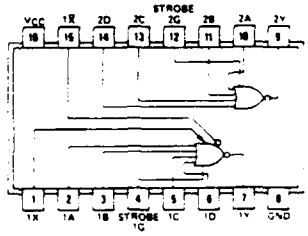
positive logic:

$1Y = \overline{1G(1A+1B+1C+1D)+X}$

$2Y = \overline{2G(2A+2B+2C+2D)}$

X = output of SN5460/SN7460

See page 113



SN5423/SN7423 (J, N, W)

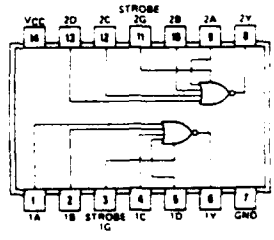
25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

$Y = \overline{G(A+B+C+D)}$

See page 92



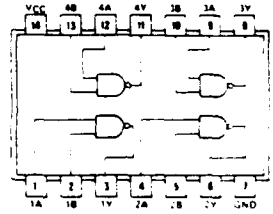
SN5425/SN7425 (J, N, W)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

26
QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 106

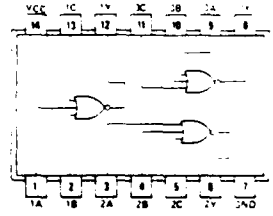


SN5426/SN7426(J, N)

27
TRIPLE 3-INPUT
POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B+C}$

See page 92

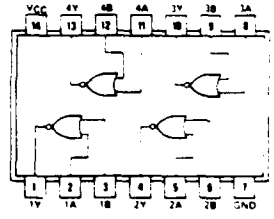


SN5427/SN7427(J, N, W)
SN54LS27/SN74LS27(J, N, W)

28
QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

positive logic:
$Y = \overline{A+B}$

See page 102

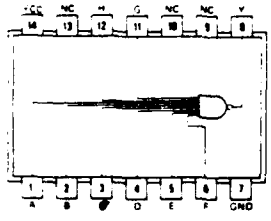


SN5428/SN7428(J, N, W)
SN54LS28/SN74LS28(J, N, W)

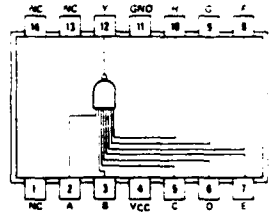
30
8-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCDEFGH}$

See page 86



SN5430/SN7430(J, N)
SN54H30/SN74H30(J, N)
SN54L30/SN74L30(J, N)
SN54LS30/SN74LS30(J, N, W)
SN54S30/SN74S30(J, N, W)



SN5430/SN7430(W)
SN54H30/SN74H30(W)
SN54L30/SN74L30(T)

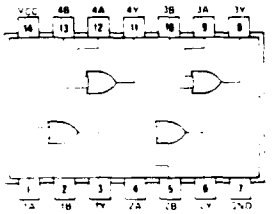
NC – No internal connection

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

32
QUADRUPLE 2-INPUT
POSITIVE-OR GATES

positive logic:
$Y = A+B$

See page 108

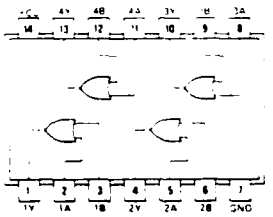


SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

33
QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A+B}$

See page 106

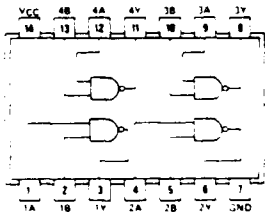


SN5433/SN7433(J, N, W)
SN54LS33/SN74LS33(J, N, W)

37
QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

positive logic:
$Y = \overline{AB}$

See page 102

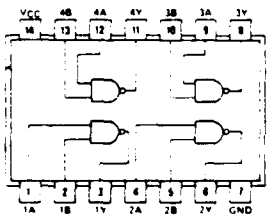


SN5437/SN7437(J, N, W)
SN54LS37/SN74LS37(J, N, W)

38
QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

See page 106



SN5438/SN7438(J, N, W)
SN54LS38/SN74LS38(J, N, W)

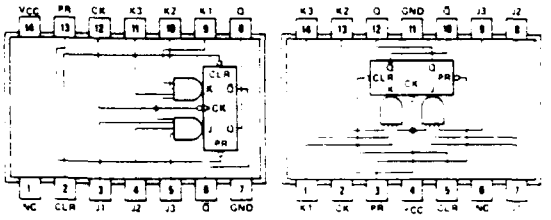
FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

72 — AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

positive logic: J = J1·J2·J3, K1·K2·K3



SN5472/SN7472(J, N)
SN54H72/SN74H72(J, N)
SN54L72/SN74L72(J, N)

SN5472/SN7472(W)
SN54H72/SN74H72(W)
SN54L72/SN74L72(T)

NC – No internal connection

See pages 120, 124, and 128

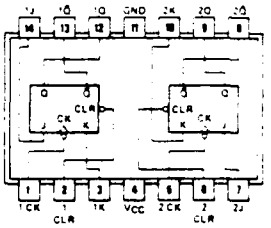
73 — DUAL J-K FLIP-FLOPS WITH CLEAR

'73, 'H73, 'L73 FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

'LS73 FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



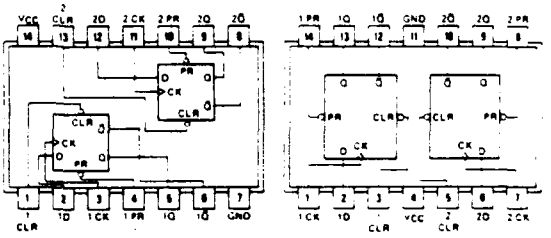
SN5473/SN7473(J, N, W)
SN54H73/SN74H73(J, N, W)
SN54L73/SN74L73(J, N, T)
SN54LS73/SN74LS73(J, N, W)

See pages 120, 124, 128, and 130

74 — DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



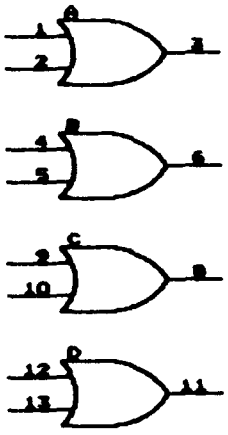
SN5474/SN7474(J, N)
SN54H74/SN74H74(J, N)
SN54L74/SN74L74(J, N)
SN54LS74/SN74LS74(J, N, W)
SN54S74/SN74S74(J, N, W)

SN5474/SN7474(W)
SN54H74/SN74H74(W)
SN54L74/SN74L74(T)

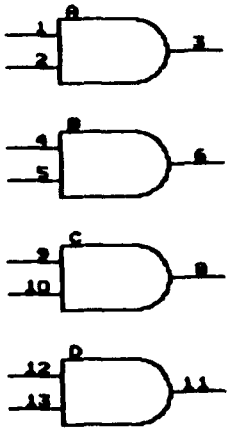
See pages 120, 124, 128, 130, and 132

H = high level (steady state), L = low level (steady state), X = irrelevant
⎍ = high-level pulse; data inputs should be held constant while clock is high, data is transferred to output on the falling edge of the pulse.
↑ = transition from low to high level, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE = Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

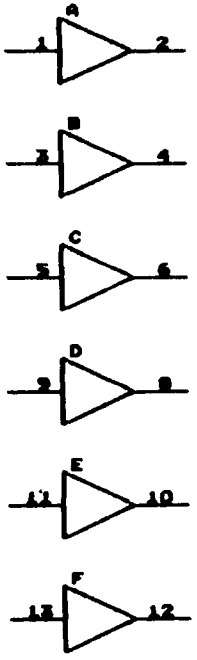
QUAD INPUT OR GATE
7432



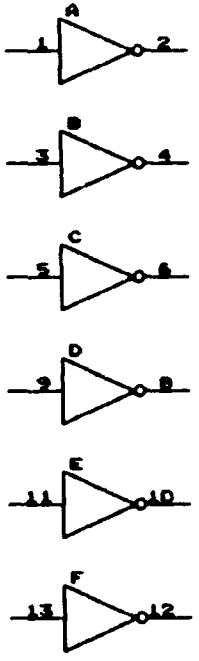
QUAD INPUT AND GATE
7408



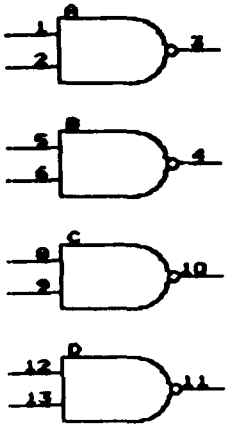
HEX BUFFER
7407



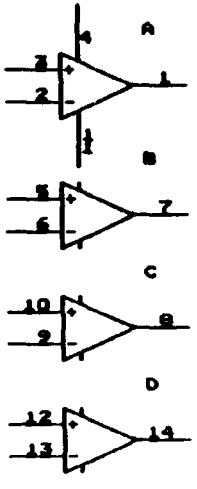
HEX INVERTER
7404



CMOS
QUAD NAND GATE
4011



QUAD ANALOG AMP
LF347D



CHIPS USED IN LOGIC PANEL		RBR SYSTEM
Size A	Document Number	REV
Date: July 17, 1991	Sheet	of